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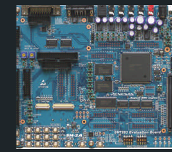

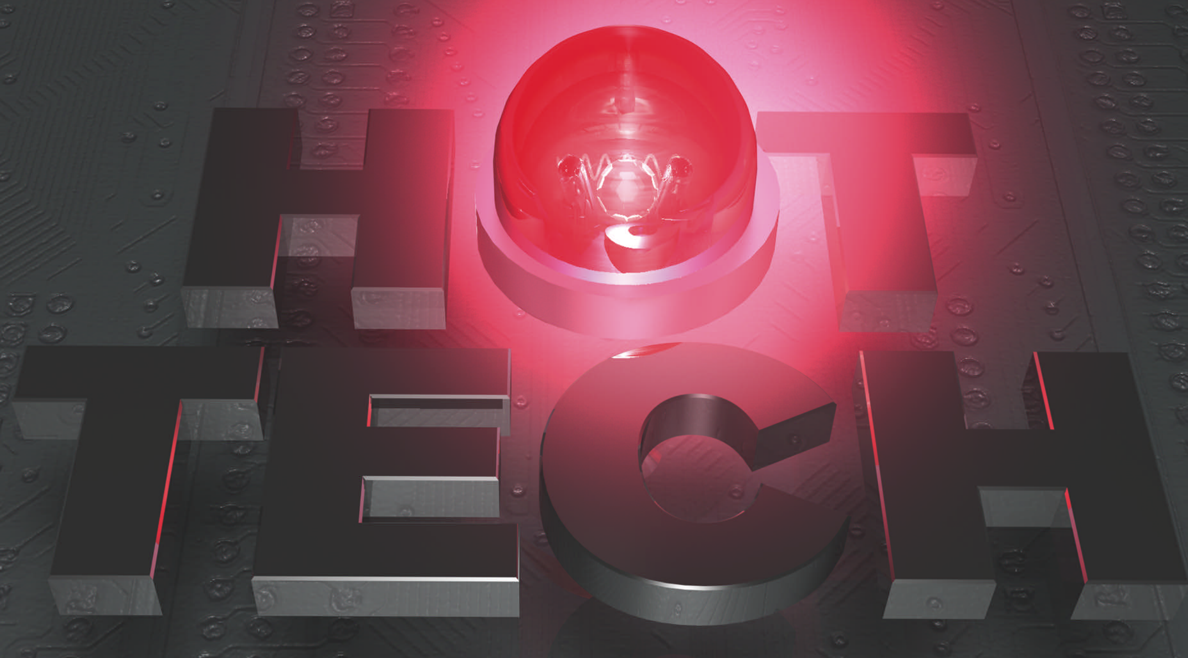

HARDWARE AND SOFTWARE APPROACHES IMPLEMENT MULTIPLE RADIOS

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ALSO FEATURING
THE HOT 100 PRODUCTS OF 2008

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AUTOMOTIVE EMBEDDED DEVELOPMENT AND TESTING

Page 46

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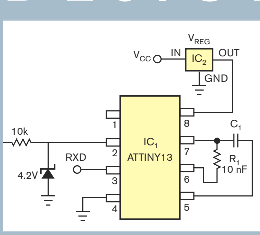

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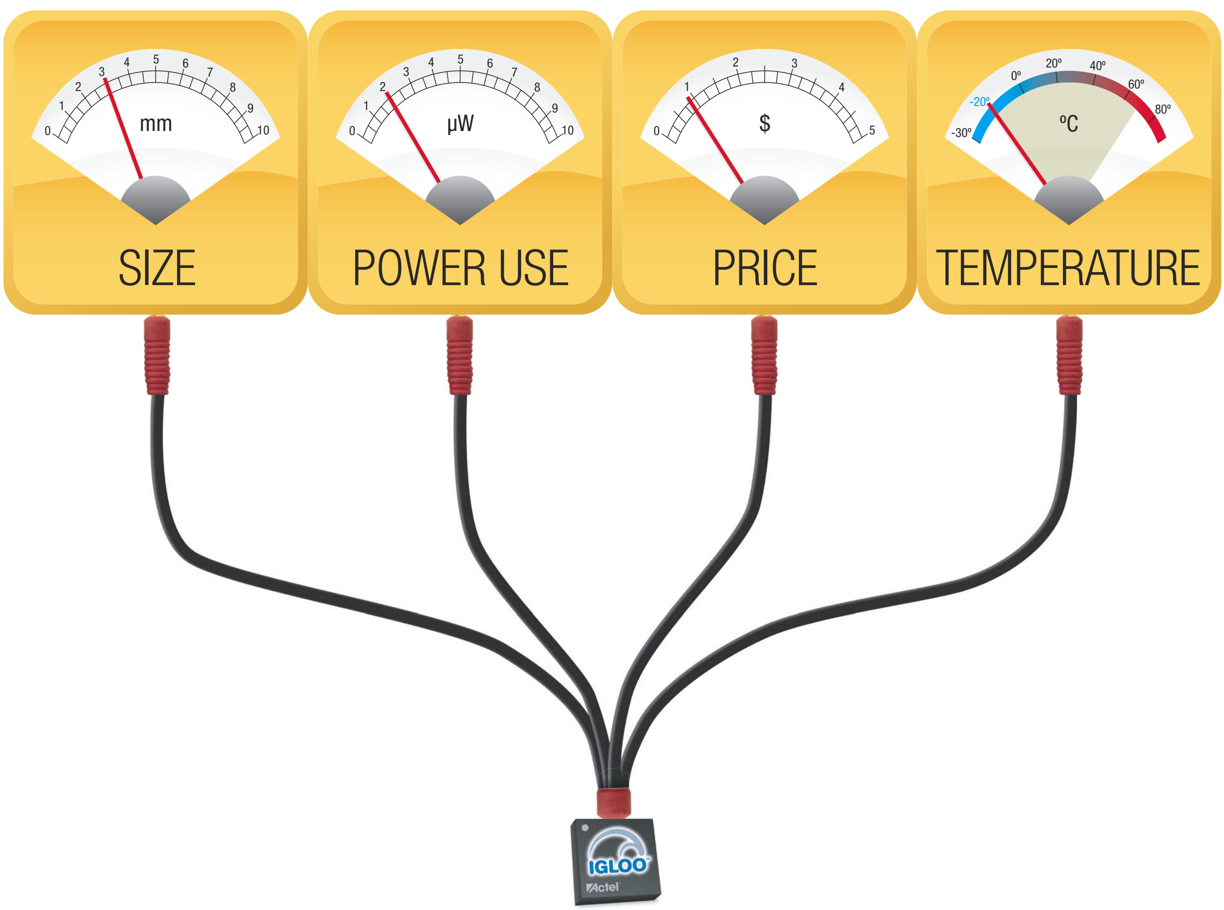

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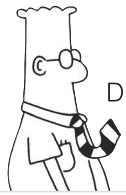

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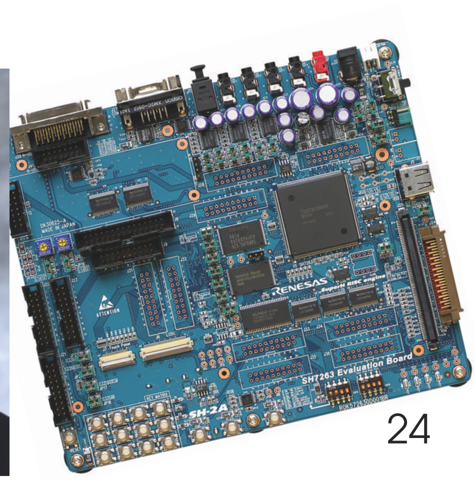

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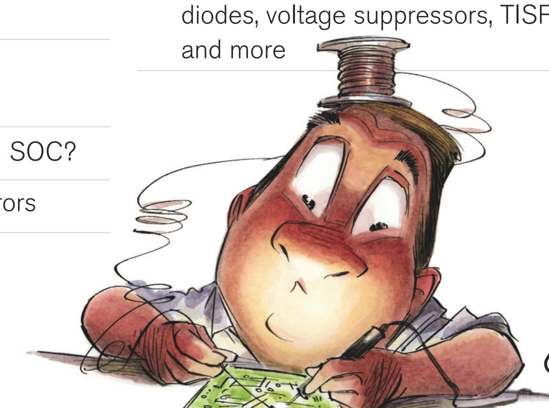
DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP



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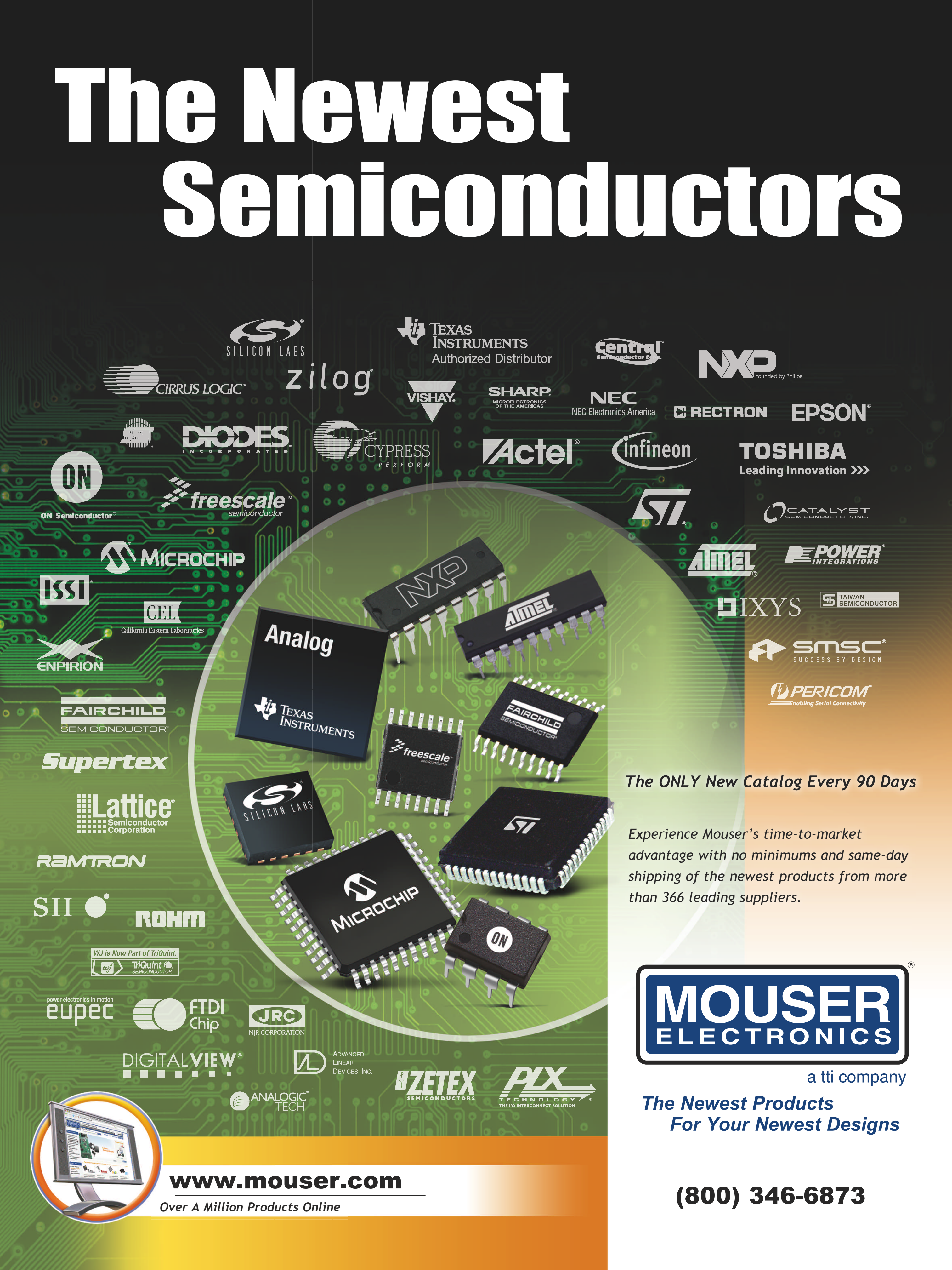

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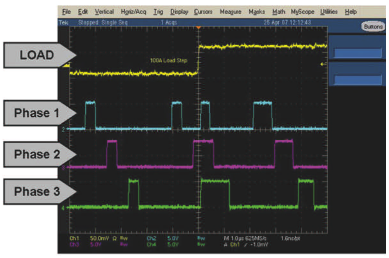

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Powering today's microprocessors: old myths versus modern technology
Five years ago, the prevailing wisdom was that multiphase buck converters switching at 1 MHz or higher would be the answer for powering tomorrow's superfast and power-hungry processors. But converter inefficiency at higher switching frequencies may force designers to consider lower-frequency dual-edge PWM (pulse-width-modulation) controllers as a better alternative.
→www.edn.com/article/CA6619540

Through-silicon vias, oxide bonding accelerate 3-D-IC development
→www.edn.com/article/CA6618763

Tips for designing ultralow-power systems
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Reducing risk by integrating configurable mixed-signal data converters
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MEMS-based inertial sensor is not your grandfather's gyroscope
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Linear wind-power meter compensates for temperature
→www.edn.com/article/CA6611644

Just use a 100Ω resistor: understanding a rule of thumb for oscillating amplifiers
→www.edn.com/article/CA6615600

Simple tester checks Christmas-tree lights

It's nine years old, and it's applicable only to a kind of holiday-light string that you'd be hard-pressed to find for sale anymore. But every year in December, this Design Idea from 1999 climbs nearly to the top of our traffic rankings. Our records show that the people viewing the article enter after Googling things like "troubleshooting Christmas tree lights" and "Christmas light testing," so we can only surmise that festive folks the world over are working hard to keep older strings of lights working rather than going out to buy new ones. In any case, the seasonal phenomenon warms our hearts as surely as chestnuts roasting or pipers piping. Happy holidays!
→ www.edn.com/article/CA46423

BY RICK NELSON, EDITOR-IN-CHIEF

Signs of optimism in economic crisis

As 2008 draws to a close amid economic turmoil, our industry is looking toward an uncertain 2009. Despite the worldwide economic crisis, year-end events that I attended provided reason for optimism.

First, Rohde & Schwarz celebrated its 75th anniversary on Nov 20, 2008, with President and Chief Executive Officer Michael Vohrer expressing confidence in the future as he reported a net revenue of 1.4 billion euros for the past fiscal year—a result comparable with that of the previous year.

In addition, levels of activity at Vision 2008 (held Nov 4 to 6 in Stuttgart, Germany) and Electronica 2008 (Nov 11 to 14 in Munich) were surprisingly high. Granted, exhibitors were committed well before the recent financial collapse, but Vision 2008 organizers said they were expecting 6500 attendees (up from 5500 in 2007), 30% of whom would travel from abroad. And Messe München International, the organizer of Electronica, released a statement saying that Electronica 2008 attendance was remarkably stable. The trade fair attracted around 2800 exhibitors and around 72,000 attendees; these figures essentially are unchanged from Electronica 2006.

That's not to say that participants in these events were sanguine about the future. Vohrer at Rohde & Schwarz cautioned that no company is immune to economic disruption, adding that his company is working to promote growth while cutting cost. Rohde & Schwarz invested 16% of its revenue in R&D and expects to grow market share in each of the four areas it serves: test and measurement, secure communications, broadcasting, and radio monitoring and radio location.

Somewhat less optimistic was Horst G Heinol-Heikkinen, PhD, board member of the machine-vision group of the VDMA (German Engineering Federation). He noted at Vision 2008 that the automotive and electronics industries represent the two largest customer groups for German machine-vision suppliers, and he estimated 1.5 and 3% declines, respectively, in orders from these two markets. Overall, he said, he expects revenues, estimated to be up 6% for 2008, to be stagnant in 2009.

If there is good news for the semiconductor industry, it's that the inevitable contraction in 2009 will be neither as deep nor as long-lasting as the 2001 downturn, says Malcolm Penn, chairman and chief executive officer of Future Horizons (**Reference 1**). He says revenues in 2009 will be down about 2%, year over year, adding that "2010 should then see a strong market rebound, driven by seasonality and the green shoots of a recovering world economy."

Based on comments at Electronica, chip makers aren't sitting by idly waiting for a rebound to occur but are actively pursuing new opportunities. Brian L Halla, chairman and chief executive officer of National Semiconductor, cited opportunities in renewable-energy, electric-vehicle, and battery-management applications as well as health care. Gregg Lowe, senior vice president for analog at Texas Instruments, said his company is developing a broad portfolio of products for medical applications and has a dedicated medical-electronics business unit that focuses on the topic.

And Robbie McAdam, vice president and general manager of Analog Devices' ASC (Analog Semiconductor Components) division, said his company is addressing medical electronics with devices such as those in its iSensor intelligent-sensor-product family, which can serve in medical-imaging equipment, prosthetics, and surgical instrumentation as well as vehicle navigation. He noted, however, that the company remains focused on its core business as it explores new application areas.

Whether you are pursuing new applications or supporting core business areas, it's important to keep in mind during the downturn that—as Vohrer intimated during the anniversary celebration—the development projects you are involved in now are critical to your company's future. **EDN**

REFERENCE

1 "Industry Downturn No. 11 Won't Be as Bad as No. 10," *Semiconductor International*, Nov 20, 2008, www.semiconductor.net/article/CA6616463.

Contact me at rnelson@reedbusiness.com.

+ Go to www.edn.com/081215ed and click on Feedback Loop to post a comment on this column.

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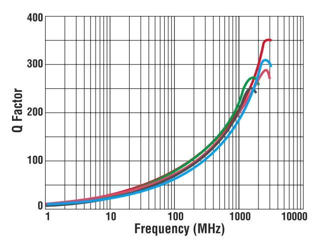
More Q. Less Cu

29
Copper
63.546

These tiny new air core inductors have the highest Q and current handling in the smallest footprint.

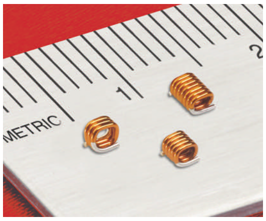
Coilcraft's new SQ air core inductors have unmatched Q factors: most are above 200 in the 1-2 GHz range! That's 3 times higher than comparably sized 0805 chip coils.



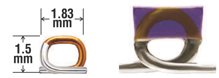
Q factors are 3X higher than standard chip inductors

And with their extremely low DCR, they can handle 4 to 8 times more current: up to 4.4 Arms.

SQ air core inductors are perfect for your LC filter and RF impedance matching applications. They come in 15 values ranging from 6 to 27.3 nH, all with 5% tolerance.



These coils are significantly smaller than existing air core inductors. We reduced the footprint by using close-wound construction and keeping the leads close to the body. The square shape cuts the height to as low as 1.5 mm and creates flat top and bottom surfaces for easy automated handling and stable mounting.



The square shape and narrow footprint reduce board space by 60-75% over conventional air core inductors.

See how the ultra-high Q and current handling of Coilcraft's new SQ air core inductors can maximize the performance of your next design. For complete specifications and free evaluation samples, visit **www.coilcraft.com/sq**

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Reed Electronics Group

LXI digitizers offer floating inputs, 128M-sample/channel memory

Agilent Technologies has introduced what it calls the first stand-alone high-resolution digitizers with LXI (local-area-network-extensions-for-instrumentation) connectivity. The company says that R&D and manufacturing engineers will choose these instruments when digital multimeters sample too slowly and oscilloscopes provide insufficient resolution for the required waveform analysis.

The two-channel L4532A and four-channel L4534A offer simultaneous sampling to 20M samples/sec with 16-bit resolution. The fully floating transformer-isolated input channels accept peak common-mode voltages as great as ±42.4V with respect to chassis and can measure full-scale signals as small as ±250 mV or as large as ±256V in such applications as electromechanical-device control for product characterization or test. There are 11 input-attenuator ranges in 2-to-1 ratios. Waveform-memory depth is 32k samples/channel with 128k samples/channel optional.

A choice of noise filters reduces the need to add expensive signal conditioning ahead of the digitizer. The units include built-in scope-like-measurement capabilities, such as maximum minimum and peak-to-peak voltage; frequency; and rise/fall time, which you can apply to selected waveform segments or to an entire waveform. The onboard measurements save postprocessing time and minimize the need to transfer and store large amounts of data.

The 1.75-in.-high, full-rack-width units fully comply with the LXI Class C specification. They include as standard features USB 2.0 and GbE (gigabit-Ethernet) interfaces, enabling quick and simple connectivity to a PC or a network. In addition, you can remotely operate the units from any browser by accessing the built-in Web page. The US prices of the two-channel L4532A and four-channel L4534A digitizers are $6500 and $8500, respectively. Extended memory for either unit adds $1500.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/lxidigitizers.

With a height of only 1.75 in., the two-channel L4532A and four-channel L4534A 16-bit-resolution LXI Class C digitizers offer a combination of features and performance you won't find in other modular ADCs.

FEEDBACK LOOP

"We have had our share of short-lived CFLs (compact fluorescent lights) and have felt that we had been sold a 'bill of goods' that turned out to be junk."

—Inventor and *EDN* reader Bill Allsopp, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6607201. Add your comments.

BUILT-UP PCB STRUCTURE EMBEDS COMPONENTS

Imbera recently announced the IMB (integrated-module-board) packaging technology, which uses conventional PCB (printed-circuit-board) materials, such as FR4, but embeds within the board many of the components that manufacturers now surface-mount. The company claims that the technology offers greater miniaturization—especially in height or profile—and improvements in certain electrical parameters.

For more information on this product, go to www.edn.com/081215pa.

—by Graham Prophet

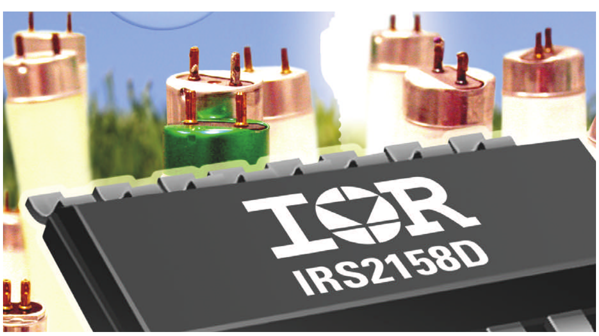
▶Imbera, www.imbera.fi.

Control ICs simplify dimming circuits for energy-efficient CFLs

Energy-efficient CFLs (compact fluorescent lights) continue to gain in popularity for home and office lighting. However, dimmer switches, which control many incandescent lights, can cause a standard CFL to break down. Dimmer switches vary the voltage to the light by switching the source ac voltage using SCRs (silicon-controlled rectifiers), thus enabling incandescent bulbs to vary their brightness from 0 to 100%.

Standard CFLs have steady 120V-ac inputs and hence do not respond well to use with dimmer switches. As a result, controlling the ballast for a CFL to adapt to the switched ac voltage requires a more complex, expensive ballast that, due to the greater number of parts and increased complexity, is more prone to failure. In addition, you cannot adjust most currently available dimmable CFLs to less than 10% of their full-on brightness.

To address this problem, International Rectifier's 600V IRS2530D and IRS2158D control ICs target CFLs that replace incandescent lights in continuously dimmable- and three-way-lighting applications. The IRS2530D DIM8 linear-dimming-ballast-control IC has a half-bridge driver and can dim a CFL to 10% of its full-on light. It is suitable for both linear ballasts and CFLs. The chip has a high-voltage pin to sense the half-bridge current and voltage in ballast-protection functions. The dc dim-input-voltage reference and ac-lamp-current feedback combine to allow the use of one pin for dimming. The combination of these high-voltage control algorithms and simple dimming method in an eight-pin IC results in fewer components, increased reliability, reduced design-cycle time, and high dimming-ballast-system performance. The IRS2530D also features an internal non-ZVS (zero-voltage-switching) and internal-crest-factor protection to prevent lamp failure from damaging the ballast.



The IRS2530D and IRS2158D 600V control ICs for energy-efficient dimmable-fluorescent-lighting-ballast applications simplify the design of dimmable CFLs and increase circuit reliability by reducing parts count.

For applications requiring dimming of less than 10%, the company offers the 16-pin IRS2158D. The IRS2158D offers additional features, such as an end-of-life window-comparator pin and an internal 60-event current-sense up/down fault counter to accommodate T5-lamp and multilamp ballasts.

The IRS2530D is available in eight-lead DIP or SOIC packages for prices starting at $1.09 (10,000). The IRS-2158D is available in 16-pin PDIP and narrow-body SOIC packages for prices starting at $1.29 (10,000). Reference-design kits are available for prices starting at $99.

—by Margery Conner

▷**International Rectifier**, www.irf.com.

DILBERT By Scott Adams

12.15.08

6-GHz SERDES CHIP CHARTS ITS OWN EYE DIAGRAM

Vitesse Semiconductor has introduced the VSC3441 SERDES (serializer/deserializer) chip. It combines a 6.375-Gbps, multirate SERDES transceiver, CDR (clock-and-data-recovery) circuitry, and Vitesse's active-equalization and VScope waveform-viewing technology. The VSC3441 operates at selected data rates of 125 Mbps to 6.375 Gbps; the advanced equalization compensates for various impairments and losses that copper cables and backplane traces and connectors cause. You can set up the equalization to match the signal paths in your design and then use VScope to verify waveforms and eye diagrams and to monitor BERs (bit-error rates) and system performance.

The multirate support targets use in next-generation backplanes and communication equipment running a variety of protocols. It can lead to a lower bill-of-materials cost when you incorporate it in a design using high-density FPGAs, according to the vendor. The VSC3441 costs $32 in volume and comes in a 196-pin, 15×15-mm flip-chip BGA package.

For more information on this product, go to www.edn.com/081215pb.

—by Graham Prophet

▶Vitesse Semiconductor, www.vscope.com.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IMEC demonstrates 3-D stacked ICs

IMEC has announced that it has made significant progress with its 3D-SIC (3-D-stacked-IC) technology, having demonstrated its first functional 3-D ICs, which it achieved by using die-to-die stacking on 5-micron copper TSVs (through-silicon vias). Engineers speaking at the IMEC ARRM (Annual Research Review Meeting) on Oct 13 in Leuven, Belgium, described the 3-D technology and outlined the design and test challenges 3-D circuits impose.

Eric Beyne, IMEC scientific director for 3-D technologies, reported that IMEC realized the die in the demonstration 200-mm wafers in IMEC's reference 0.13-micron CMOS process with an added copper-TSV process. For stacking, the research organization thinned down the top die to 25 microns and bonded it to the landing die using copper-to-copper thermocompression. IMEC is upscaling the process for die-to-wafer bonding and is on track for migrating the process to its 300-mm platform.

To evaluate the impact of the 3D-SIC flow on the characteristics of the stacked layers, both the top and the landing wafers contain parametric-test structures for TSV characterization; CMOS-ring oscillators; and other small, functional circuits. Tests confirmed that the performance of the circuits does not degrade when copper TSVs are added and the die are stacked.

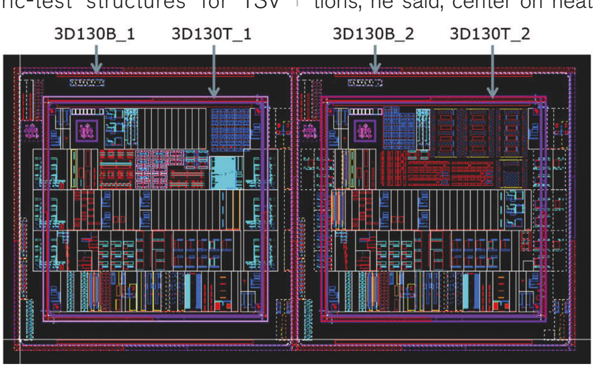
Also speaking at the ARRM, Pol Marchal, principal scientist at IMEC working on all aspects of design of digital systems, with a special emphasis on 3-D design and technology-aware design techniques for low-power systems, described the design and test challenges that 3-D structures impose. To extract value from 3-D, he said, engineers must rethink system architectures, employing a physically aware system-exploration approach. Questions engineers face range from partitioning (where, for example, to put memory, logic, and RF functions) to test—that is, whether to use BIST (built-in self-test) or JTAG. Other questions, he said, center on heat dissipation, manufacturability, and reliability.

> "Quiescent-current tests on the ICs may be effective ways to screen out bad die at the wafer level.

Marchal proposed the use of IMEC's PathFinding virtual-design flow to help explore the physical-design impact of various design options. The PathFinding flow works with TCAD (technology-computer-aided-design) models and a set of virtual-design rules to provide spatially aware estimates of performance and power. He concluded by describing a 3-D stacked-DRAM implementation for fine-tuning IMEC's technology and for demonstrating the feasibility of 3-D design.

The IMEC 3-D approach presents some test and reliability challenges that are largely absent from 2-D ICs or traditional multichip packages in which wire bonds interconnect the die. Beyne pointed out that the die must be "singulated," a process that can generate potentially troublesome particles. (With modern 2-D approaches, process variation—not particle contamination—can cause the most problems.) The requirement for singulation complicates the known-good-die problem—the difficulty of ensuring that each die in a multidie package is good before package assembly. Beyne noted that most 3-D approaches would probably involve die-on-die or die-on-wafer fabrication; wafer-on-wafer fabrication, he said, would result in too many good die mated to bad ones. Beyne said that quiescent-current tests on the ICs may be effective ways to screen out bad die at the wafer level; manufacturers could then defer full-test coverage until final multidie-package testing.**—by Rick Nelson**

▷**IMEC**, www.imec.be.



IMEC developed a test chip for assessing design rules and models for its 3D-SIC technology.

12.15.08

PROCESSOR SPORTS EVENT SYSTEM

Atmel's 8/16-bit ATXMega A3B microcontroller combines an eight-channel event system with a four-channel DMA controller that simultaneously manages eight interperipheral signals and as many as four 64-Mbps data communication channels. The device accomplishes these tasks at 32 MHz without any CPU intervention and at a power draw of 12 mA, not including CPU activity. The event handler allows the system to avoid software-managed context switching and interrupt handling. An event consumes less than 10 nA, and event-response time is as fast as 31.25 nsec. The maximum guaranteed response time of an event is two clock cycles, or 62.5 nsec with a 32-MHz system clock.

The software-configurable XMega event system manages autonomous triggers for peripheral-to-peripheral interactions using timer/counter-compare-match-or-overflow, analog-comparator toggle, pin-change, ADC-complete-or-compare, and real-time-counter-overflow events.

Several XMega devices are available immediately with 64 to 256 kbytes of flash memory in 64- or 100-pin packages for $3.12 to $3.55 (10000).

For an expanded version of this item, go to www.edn.com/article/CA6609829.

—by Robert Cravotta

▶Atmel, www.atmel.com.

VOICES

Microchip's Ganesh Moorthy

Ganesh Moorthy is the executive vice president at Microchip Technology, which manufactures microcontroller, memory, and analog semiconductors. The company's products include the PICmicro and dsPIC/PIC24 microcontrollers; serial-EEPROM, Keeloq, RF, thermal, power, and battery-management analog devices; and linear, interface, and mixed-signal devices. Moorthy recently spoke with *EDN* about supporting embedded developers. An excerpt of that interview follows. For the full interview, go to www.edn.com/081215pb.

Microchip has broadened its processor portfolio to span from 8- to 32-bit processors, including microcontrollers and digital-signal controllers. What is Microchip's strategy for supporting this range of architectures?

A Our strategy is to offer a broad range of microcontrollers across the 8-, 16-, and 32-bit architecture ranges. We continue to hear feedback from our customers that this [range] is what they want, and we continue to innovate for each of these architecture points. The reason for this [offering] is that, in the embedded space, the needs of a customer are quite fragmented, and it is important to have a number of products that can all solve any one problem to enable the customer to pick and choose as they go through a design and identify their real system requirements—the final product that meets the exact system requirements.

Our own experience says that, in as much as 70 to 80% of designs, the product the customer goes to production with is different from the product they begin the design development on. The reason for this [difference] is that, during the time frame that they are conducting the design, the customers [have the time] to better refine their system requirements. They are able to appropriately adjust on the fly to new needs identified by their sales and marketing teams to make their end product more competitive and to be able to do all of this in some seamless fashion. So, they do not have to throw away all of their engineering effort each time they need to make a change. The ability to shift to the next appropriate product—whether for cost, size, features, or whatever is driving the change—is a very powerful need. Having a broad portfolio of products spanning 8, 16, and 32 bits is intended to offer that breadth of choice, no matter how their needs are changing.

How does Microchip address balancing general-purpose and application-specific processing?

A Almost all of our products could be considered general-purpose products. Now, we do take many of them and give them an application twist, so to speak. For some of the products, we will add peripherals that are more fine-tuned to running specific applications, such as for motor control or touch sensing, or add some communication protocol, such as CAN [controller-area networking], USB, or Ethernet. Fundamentally, the products are broad-based, and then we take one or more dimensions where we give it a little more personality for a particular application without impeding its use in other applications.

The goal is to make it a low-risk effort to enter a design and get to production without having to rework the software and the best total cost implementation for the application. The PIC platform is a singular common platform that supports development across the entire line of 8-, 16-, and 32-bit products with an integrated development environment, assemblers, other software, and hardware debugging for emulation. The 32-bit controllers are upgrades from the 16-bit controllers.

Besides growing computational-processing capabilities, what other capabilities do you see being integrated with embedded processors? How are these features helping to drive innovation?

A In the area of analog, we have a significant amount of analog integrated onboard, such as oscillators to avoid needing external oscillators, brown-out-resets, as well as ADCs and DACs. Then, we have added more traditional peripherals, multiple UARTs, multiple I^2Cs [inter-integrated circuits], multiple SPIs [serial-peripheral interfaces], as well as hardware modules to help handle software protocols, such as LIN [local-interconnect network], that can run off a standard UART, but, if the UART has additional hardware features, it is easier to implement the protocol. We've added the capability of adding a touch peripheral to our products without the need for external components.

There is a range of communication peripherals, USB and USB On-The-Go communication, as well as Ethernet MAC [media-access-control] and PHY [physical] layers integrated onboard. The peripheral-pin select allows customers to remap pins to whatever I/O they want, so they can fit [the design] into smaller packages and use more intelligent routing on their boards.

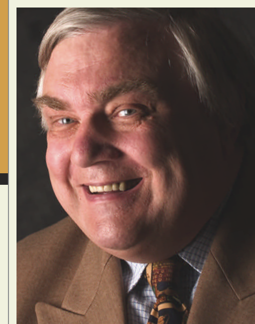
Our focus is on the innovation that customers want to apply and the flexibility they want to have in what they do. We try to enable innovation. At any given point, customers are thinking about what innovation means to them, and, at one point, it may mean getting to lower cost or smaller size or being able to implement something, like touch sense, that they couldn't implement before. In the end, we want to enable our customer's innovation.

—Interview conducted and edited by Robert Cravotta

RAQs

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices



Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

How Big Is It?

Q. How can I handle signals with huge variations in amplitude?

A. With a Logarithmic Amplifier.

The world's smallest mammal is the Etruscan Pygmy Shrew, which is about 3 cm long (plus tail) and weighs less than 1.5 gm (that's 20 to the ounce - one tenth the size of a mouse). The largest, the Blue Whale, can be over 30 meters in length and over 150 tons or thirty times the size of an elephant in weight. That's a thousand times longer and more than one hundred million times heavier than the pygmy shrew.

It is easy to measure small things and equally easy to measure large ones but when it is necessary to measure both, matters become complex. The ratio of the smallest and the largest signal that a system can handle is known as its "dynamic range" and is usually expressed in dB. A system where the largest voltage or current is a thousand times the smallest has a dynamic range of 60 dB, for a million times the figure is 120 dB.

We need a 28-bit digital system before an LSB is less than 1/100,000,000 of an MSB so a digital system that must handle such variation needs either very high resolution, or complex signal processing.

But some analog circuits can easily handle very large dynamic ranges. These are known as "logarithmic amplifiers" (log amps) or, more properly but less commonly, "logarithmic converters." The output of a log amp is proportional to the logarithm of the input. Some log amps can handle dynamic ranges of over 160 dB.

There are a number of different log amp architectures. Some, which use the log properties of silicon junctions, have a very large dynamic range but low speed, others (successive detection log amps), which use cascaded detector/amplifiers to create a log response, can be made with bandwidths of many GHz and still have an accurate log response over a dynamic range of 60 to 90 dB.

Both types can be made as integrated circuits. The linked article describes their various structures and properties in more detail. They are easy to understand and easy to use, but are not often discussed in basic textbooks, so they are often overlooked by inexperienced analog designers.

Wherever systems must handle very large analog signal ranges, engineers should consider the use of log amps. They are simple, affordable, and ***very*** useful.

To learn more about logarithmic amplifiers,

http://designnews.hotims.com/22339-101

Have a question involving a perplexing or unusual analog problem? Submit your question to:

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ANALOG DEVICES

BY BONNIE BAKER

What's in your SAR-ADC application?

"Finding an amplifier that doesn't tarnish an ADC's performance is hard enough. But now you also have to deal with single-supply voltages and the quirky switched-capacitor input structure" (**Reference 1**). Engineers have been struggling with the task of driving the SAR (successive-approximation-register)-ADC, charge-redistribution, or C-DAC (capacitive-data-acquisition-converter) input architectures for more than a decade.

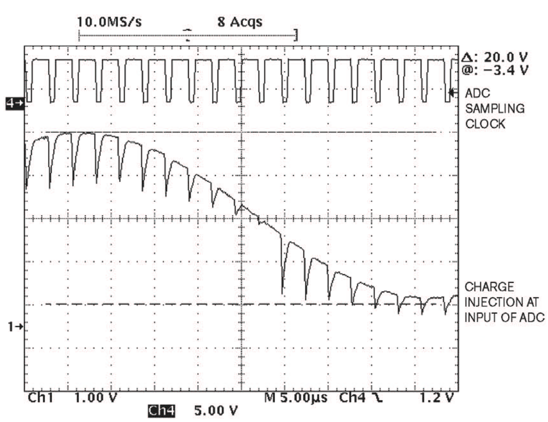

Figure 1 By placing a 10-kΩ resistor between a buffer op amp and a SAR-ADC input, you can see the ADC charge-injection action.

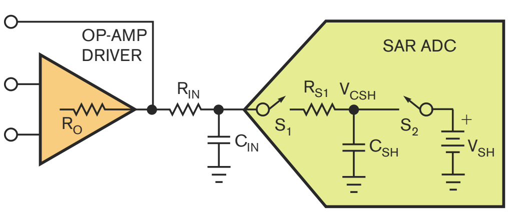

Figure 2 Choose an amplifier with an input range that is appropriate for the input-signal requirements, then connect the amplifier through an RC system to the ADC.

Driving a SAR ADC with an amplifier seems like a simple task. You choose an amplifier with a bandwidth that is appropriate for the input-signal requirements, then connect the amplifier directly to the ADC as a buffer. Not so fast. You are not finished until you accommodate the effects of the ADC-input charge injection on your amplifier (**Figure 1**). The transient currents at the input of the SAR ADC can disrupt the output of the amplifier so that the conversion process produces inaccurate digital results.

You model the input structure of the SAR ADC with a switch to an input capacitor, C_{SH}, to ground (**Figure 2**). Prior to signal acquisition, the ADC S_2 switch connects the power supply, voltage reference, or ground to precharge C_{SH}. Your particular ADC topology determines this precharged voltage value. At the start of the signal-acquisition time, S_2 opens and S_1 closes. When S_1 closes, the system injects charge onto or off of C_{SH}, and the ADC takes a predetermined amount of time to acquire the signal. During this signal-acquisition time, the ADC requires ample charge from an input source to bring the system within a ½-LSB accuracy window.

To design your circuit to perform accurately with the first pass, insert a resistor, R_{IN}, and a capacitor, C_{IN}, in the signal path between the amplifier and the ADC (**Figure 2**). The capacitor serves as a charge reservoir providing ample charge to the input capacitor of the ADC. R_{IN} isolates the amplifier from C_{IN} and stabilizes the amplifier (**Reference 2**). The combination of R_{IN} and C_{IN} at least needs to meet the ADC's acquisition time (**Reference 3**). Finally, select your amplifier bandwidth to match the $R_{IN}C_{IN}$ time constant.

If you design your SAR-ADC circuit by simply driving the input of the converter with an amplifier, it may not produce good results. If you insert an RC pair between the amplifier and the SAR ADC, you will successfully charge your converter and design the quirks out of your circuit from the start. **EDN**

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Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

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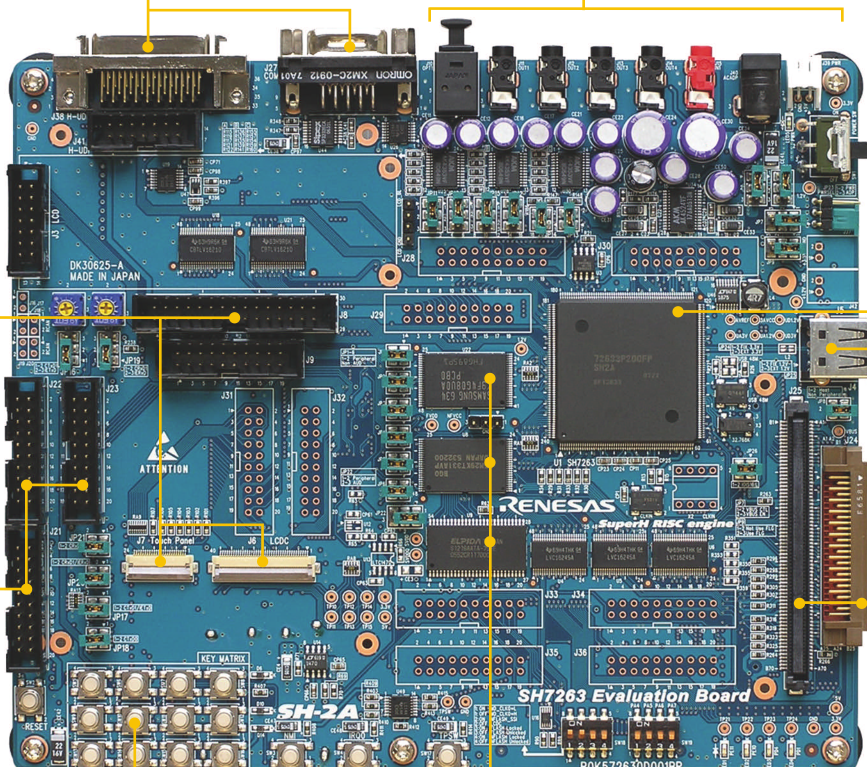
When is a microcontroller an SOC?

It's getting harder and harder to tell the difference between a microcontroller and an SOC (system on chip). Consider, for example, the SH7263 portable-media-player reference design from Renesas. It offers all the latest features, including a VGA (video-graphics-array)-level LCD, high-speed USB (Universal Serial Bus) and SD (secure-digital) interfaces, and decoders for a wide range of audio standards. Renesas is considering the addition of an MPEG-4 video decoder, as well. Surprisingly, the company based this design on the SH-powered 7263 microcontroller chip rather than on a proprietary multimedia SOC. The microcontroller core, offering performance greater than 400 Dhrystone MIPS, has the muscle for media decoders in software, and the chip includes controllers for high-speed USB 2.0 and a WVGA (wide-VGA)-display panel. That combination leaves not much but the mixed-signal interfaces, the audio DACs, and the power supply as separate components.

The SH7263 microcontroller has a 16.67-MHz input clock, a 66.67-MHz-maximum bus clock, and a 200-MHz-maximum CPU clock.

The E10A package includes the proprietary AUD (Advanced User Debugger) interface. Jumper switches let you select the AUD function. The device also includes a serial interface.

Audio DACs and a power supply are the only major functions not integrated into the microcontroller.



A WVGA-level LCD supports resolutions as high as WVGA–that is, 640×480 pixels with a 1.78-to-1 aspect ratio.

USB support includes high-speed capability.

The signal headers reside below the LCD panel.

Connectors support the chip's external expansion bus and ATAPI (advanced-technology-attachment packet interface) port.

A 3×4 user switch matrix is scanned by the microcontroller.

The SD-card slot resides on the underside of the board.

In addition to on-chip memory, the board includes a 512-Mbyte NAND flash, a 4-Mbyte×16-bit flash, and a 16-Mbyte×16-bit SDRAM.

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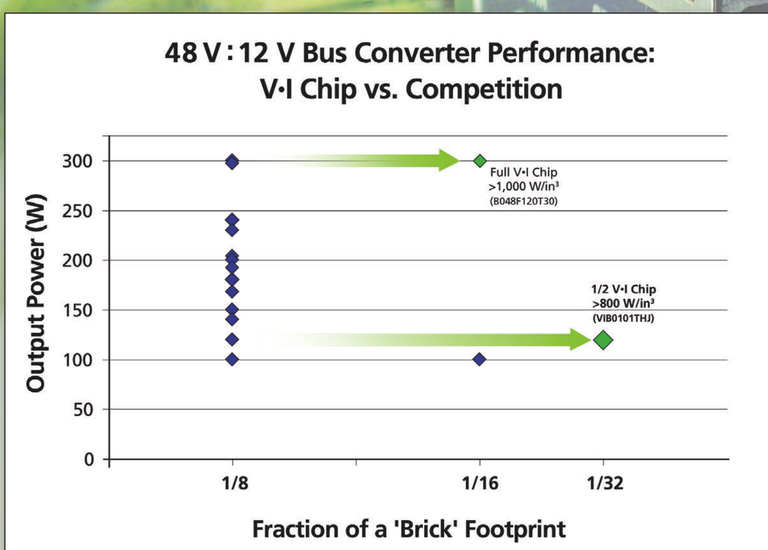

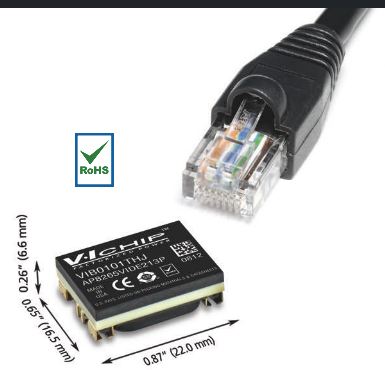

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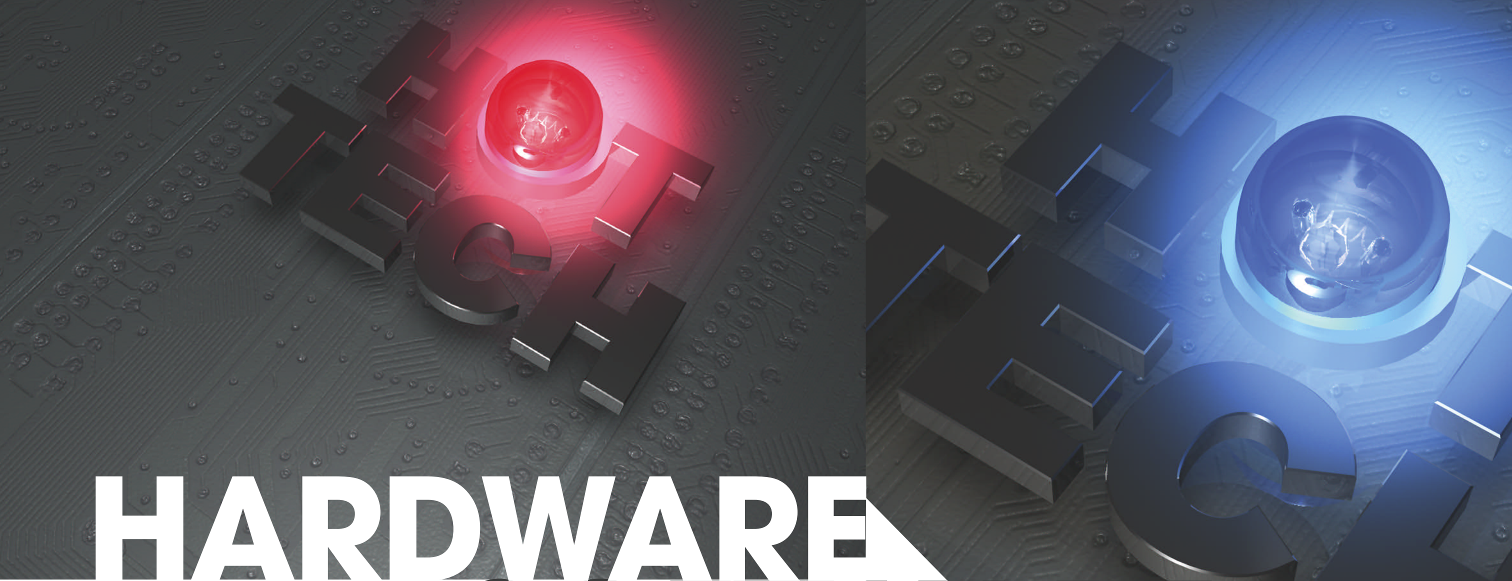

HARDWARE AND SOFTWARE APPROACHES IMPLEMENT MULTIPLE RADIOS

BY RICK NELSON • EDITOR-IN-CHIEF

MINIATURIZATION AND EMERGING FLEXIBLE SOFTWARE ARCHITECTURES WILL ENABLE COMPACT, LOW-POWER WIRELESS DEVICES TO SUPPORT COMMUNICATIONS STANDARDS RANGING FROM BLUETOOTH TO WIMAX.

Today's on-the-go consumers may think they are carrying a single cell phone, but they're actually carrying seven or more radios that handle multiband-cellular operation, Wi-Fi networking, Bluetooth connectivity, assisted-GPS (global-positioning-system) functions, and more. In the future, they might have radios that implement ad hoc device-to-device communications, in which one device takes advantage of a nearby device that has better coverage (see **sidebar** "Ad hoc sharing could mean more radios"). To fit all the necessary radio functions into a portable wireless device, researchers throughout 2008 have been developing miniature multifunction modules and exploring flexible, low-power SDR (software-defined-radio) architectures.

The traditional way of implementing multiple radios in a single product is simply to design in multiple discrete radios—a transmit/receive function for each communications standard your product aims to support. That approach can take up a lot of real estate, a problem that Epcos addresses with its miniature front-end LTCC (low-temperature-cofired-ceramic)-radio modules. "We ship … a fully tested RF system in a single package," says Patric Heide, PhD, the company's director of product development for modules. "In a mobile phone, you have the CMOS-based radio IC built in on one side, and, on the other side, you have the antenna. We provide a fully featured front-end module that goes between the two." To shrink multiple-radio implementations, Epcos offers multiradio modules, such as a Wi-Fi/WiMax (worldwide-interoperability-for-microwave-access) module (**Figure 1**). See **Reference 1** for a discussion on how to test the modules.

Modules such at the Epcos LTCCs can accommodate semiconductor components such as GaAs (gallium-arsenide) power amplifiers, but the CMOS-radio chips that accompany the front-end modules in the transmitter/receiver-signal chain embody many of the radio functions. You can use multiple CMOS chips to implement multiple radio standards. A more elegant approach involves using one flexible CMOS chip to implement multiple radio standards.

Justin R Rattner, vice president and chief technology officer of Intel, addressed that topic last June at the Design Automation Conference in Anaheim, CA (**Reference 2**). In a keynote speech, "EDA for digital, programmable multi-radios," he noted that consumers want to "carry small yet live large"—that is, they expect compact designs to have multiple advanced features. To support this carry-small/live-large lifestyle, consumer devices must support "anywhere/anytime" collaboration, with the device able to communicate no matter what air interface—3G (third-generation) cellular, Wi-Fi, or WiMax, for example—is available.

Rattner acknowledged that we live in an analog world. "Analog is how we interact with the real world, but the technology favors digital," he said. "So, we have to bridge the gap between the analog world and the digital world." Bridging this gap will be important for the carry-small/live-large lifestyle. He further acknowledged that the amount of analog circuitry is increasing: In 2006, more than 70% of SOCs (systems on chips) had analog elements. Unfortunately, however, traditional analog development is not getting any easier in the face of transistor scaling. The reasons for this difficulty are increased mask costs; leakage and process-variation effects; output impedance; increased flicker noise; and reduced supply voltages, which decrease dynamic range.

AT A GLANCE

- Consumers want to "carry small yet live large"–that is, they expect compact designs to have multiple advanced features.
- "Digitally assisted analog" turns an analog problem into a digital one by relying on digital gates to improve analog performance.
- A cognitive radio can autonomously change its parameters based on interaction with the environment in which it operates, and it coexists with and uses the same spectrum.
- Industry watchers predict that radios' ADCs will move ever closer to their antennas, yielding an intuitive, flexible full cognitive radio by approximately 2030.

His inclination is to employ "digitally assisted analog"—turning an analog problem into a digital one by relying on digital gates to improve analog performance. The technique exploits the computational nature of radio, which information theory embodies, to dramatically simplify radio architectures; to allow one radio to simultaneously act as many to, for example, facilitate seamless handoff between 3G and Wi-Fi networks; and to investigate the radio environment to see whether higher-performance networks are available.

In Rattner's version of a digital-multiradio implementation, the traditional analog-receiver-signal chain, comprising a front-end module, a mixer, and a channel-select filter, for example, gives way to a simplified digital approach. Single chips can now implement a Wi-Fi or 3G radio. Tomorrow will bring integrated, programmable multiradio implementations to deal with any air interface they encounter. According to Rattner, Intel will probably need a year or so to produce commercial versions of such a digital radio, but the company has built a digital power amplifier in 65-nm CMOS and a fractional-N synthesizer in 90-nm CMOS.

An organization that's far along in this effort is IMEC, which, at its Annual Research Review Meeting on Oct 14, 2008, in Brussels, Belgium, demonstrated an SDR platform. Liesbet Van der Perre, scientific director of

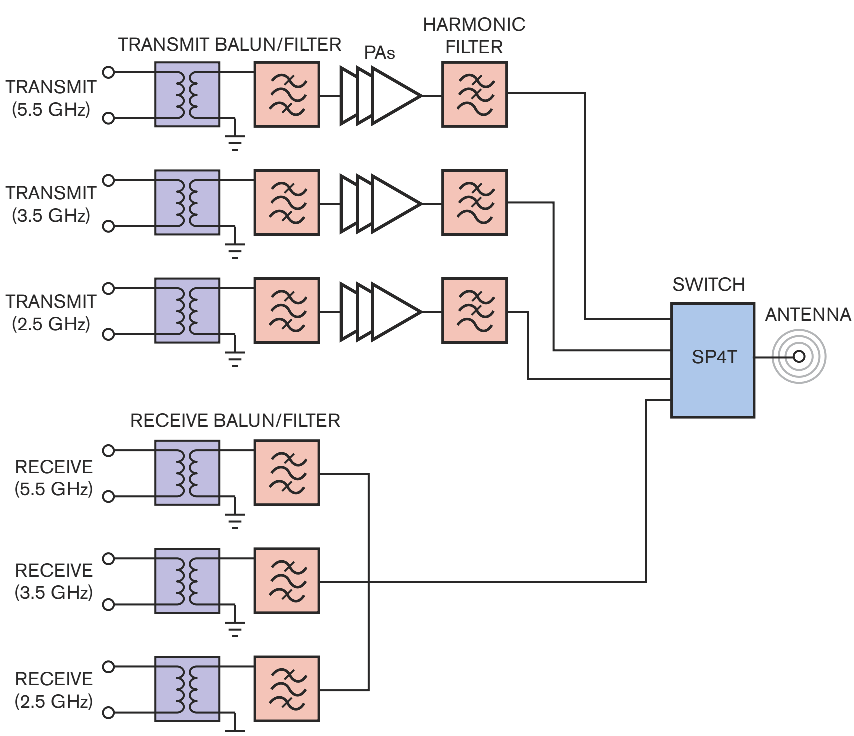

Figure 1 An Epcos triband front-end module, implementing 2.5- and 3.5-GHz WiMax as well as 2.5- and 5.5-GHz Wi-Fi, includes baluns, filters, power amplifiers, and an SP4T (single-pole/four-throw) switch on the RF-tested LTCC substrate.

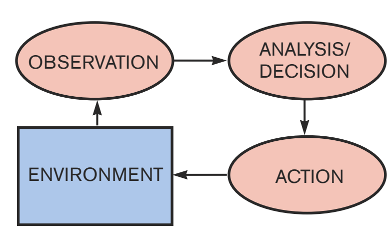

Figure 2 A cognitive radio can autonomously change its parameters based on interaction with the environment in which it operates.

wireless research at IMEC, says that the organization's SDR prototype integrates key components for next-generation flexible mobile terminals. The prototype incorporates an RF-transceiver and programmable-baseband platform, enabling the measurement of the performance and power consumption in real-life conditions and for different operating modes, she says.

Van der Perre reports that IMEC's flexible RF transceiver front end, SCALDIO (scalable radio chip), operates with all current and future cellular, WLAN (wireless-local-area-network), WPAN (wireless-personal-area-network), broadcast, and positioning standards in the 174-MHz to 6-GHz frequency range. IMEC's programmable-

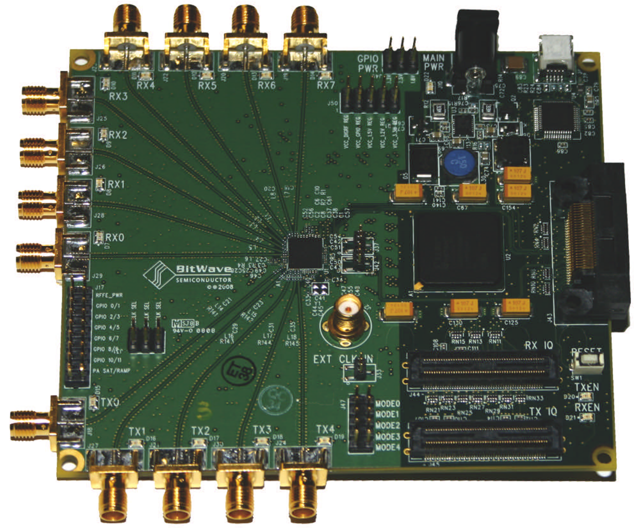

Figure 3 An evaluation board provides access to the RF and digital sections of the BitWave RFIC so engineers can evaluate them in preparation for commercial release.

AD HOC SHARING COULD MEAN MORE RADIOS

If you have a mobile wireless consumer device, you probably know what radios it contains based on the functions you purchased. It might support multiband-cellular operation, for example, as well as Bluetooth, GPS (global-positioning-system), and Wi-Fi connectivity. In the future, however, you might carry a handset that includes stealth radios whose only function is to piggyback other neighboring devices to provide access to, for example, a clear GSM (global-system-for-mobile-communications) signal.

The US military has championed this technique, ad hoc networking, as a way to enhance communications in hostile environments, according to John Irza, technical-marketing manager at The MathWorks. Izra cites, for example, a first responder entering a damaged subway tunnel. The responder would quickly lose contact with the terrestrial-radio infrastructure but would maintain contact with the responders behind him, whose devices, in turn, can appropriately relay his signal.

Researchers at the NIST (National Institute of Standards and Technology) successfully demonstrated a prototype approach to maintaining two-way communications with first responders as they make their way in building fires and mine and tunnel collapses. These disasters and others in enclosed environments are often rife with radio dead spots and conditions that can severely weaken signals.

NIST researchers demonstrated an ad hoc system in August in conjunction with the 2008 Workshop on Precision Indoor Personnel Location and Tracking for Emergency Responders at Worcester Polytechnic Institute in Worcester, MA. At the workshop, they demonstrated a "breadcrumb-communication system" that advises first responders where to place relay devices that can extend the communications range. The NIST system makes decisions based on signal strength and eliminates the drawbacks of static approaches that require the deployment of the relays–or "breadcrumbs"–at specific distance increments without regard to environmental factors.

The ad hoc technique may also find consumer applications. Speaking at the June IEEE MTT-S International Microwave Symposium in Atlanta, Mike Farmwald, director of Skymoon Ventures, suggested an approach in which communication moves from a cell phone to a tower model to a cell phone to a cell phone to a tower to an access-point model (Reference A). Cell phones could cooperate using a side channel, allowing one phone with a poor connection because of in-building loss, for example, to get help from a phone near a window 20 feet away. Two phones cooperating would experience a 3-dB improvement in SNR (signal-to-noise ratio), he said, and an ac-operated station without a user interface and near a window could yield a 15-dB improvement. Further, such a system could significantly reduce transmitting power.

Farmwald believes that the concept could be a win for all concerned: Consumer cell phones would have better connections, fewer dropped calls, and longer battery life, and carriers could double their bits-per-second-per-hertz performance with no changes to their infrastructures. Farmwald warned, however, that, even though the technology is not complex, the politics are. Wireless carriers, he noted, would need to drive a new generation of cell phones with side-channel capability–such as 1.9-GHz DECT (digital-enhanced-cordless telecommunication)– and carriers would need to adopt a universal standard for communication and authentication to address billing issues, for example.

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baseband platform—BEAR (baseband engine for adaptive radio)—supports standards such as 802.11n, 802.16e, and mobile TV, and it is forward-compatible with the upcoming 3GPP-LTE (Third Generation Partnership Project/Long-Term Evolution communication) standard.

The connectivity-centric SDR platform makes flexible and efficient use of network and spectrum resources across heterogeneous environments. SDR also serves as an enabling technology for spectrum-centric, opportunistic, cognitive-radio applications. A cognitive radio (**Figure 2**) can autonomously change its parameters based on interaction with the environment in which it operates, and it coexists with and uses the same spectrum resources as other wireless systems without introducing significant levels of interference. Full cognitive radio won't be available until 2025 or 2030, Van der Perre estimates, but evolutionary cognitive-radio features—that SDR implementations enable—will become available in the interim.

As for SDRs, companies dedicated to the concept include Vanu, which applies the technology to base stations to enable them to simultaneously operate GSM (global-system-for-mobile) communications, CDMA (code division/multiple access), and Motorola's IDEN (integrated digital enhanced network), for example. Another is BitWave Semiconductor, whose engineers have developed an SDR IC that can morph itself to work with at least 16 wireless-network interfaces, including GSM, WCDMA (wide CDMA), Wi-Fi, WiMax, and UMTS (universal-mobile-telecommunication-system) LTE. BitWave in early 2007 released the first prototypes of the device, the Softransceiver RFIC (radio-frequency integrated circuit). The IC is now nearing commercial release, with engineers testing the devices (**Figure 3**) and characterizing them in production volumes (**Reference 3**).

IMEC announced in October that Toshiba had licensed IMEC technology applicable to SDRs. And IMEC and Panasonic last month signed a joint-research contract concerning technologies in the semiconductor, networks, wireless, and biomedical fields. Under the terms of the contract, research will take place at IMEC's Leuven, Belgium, facilities and research unit at Holst Centre in Eindhoven, the Netherlands. Part of the research will focus on dynamically reconfigurable SDRs.

John Irza, technical-marketing manager at The MathWorks, speaks from his company's vantage point as a supplier of baseband- and RF-simulation tools for chip and system vendors. He estimates that bandwidth users employ only 15 to 20% of available spectrum at once, leaving plenty of room for a cognitive radio to operate. Cognitive radio must, however, be agile enough to defer to the primary user of the spectrum when that user wants access to the spectrum that cognitive radio has appropriated. Irza notes that cognitive radio's challenges are both political and technical, requiring the approval of regulating bodies such as the Federal Communications

Commission in the United States. Thus far, the FCC has supported the cognitive-radio concept.

As for the future, Irza sees a trend toward integrated baseband/upband devices that support Bluetooth, Wi-Fi, GPS, and LTE communications standards as vendors overcome the challenges of moving digital-signal-processing functions closer to the antenna. IMEC's Van der Perre cites figures from researcher ARCchart, which optimistically predicts that manufacturers will ship 157 million SDR-enabled handsets—or 11% of all handsets—in 2011. The researcher's pessimistic forecast is 74 million SDR-enabled handsets for the same year.

Van der Perre doesn't cite figures for SDRs or cognitive radios beyond 2011, but she does predict that radios' ADCs will move ever closer to their antennas, yielding an intuitive, flexible full cognitive radio by approximately 2030. As a step toward that goal, IMEC presented at the IEEE Asian Solid-State Circuit Conference in November in Fukuoka, Japan, a 2.4-GHz sigma-delta ADC it fabricated in 90-nm CMOS. Research at IMEC continues on a scalable energy-efficient spectrum-sensing engine that could bring cognitive radio yet another step closer. **EDN**

FOR MORE INFORMATION

ARCchart
www.arcchart.com

BitWave Semiconductor
www.bitwavesemiconductor.com

Epcos
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IEEE Asian Solid-State Circuit Conference
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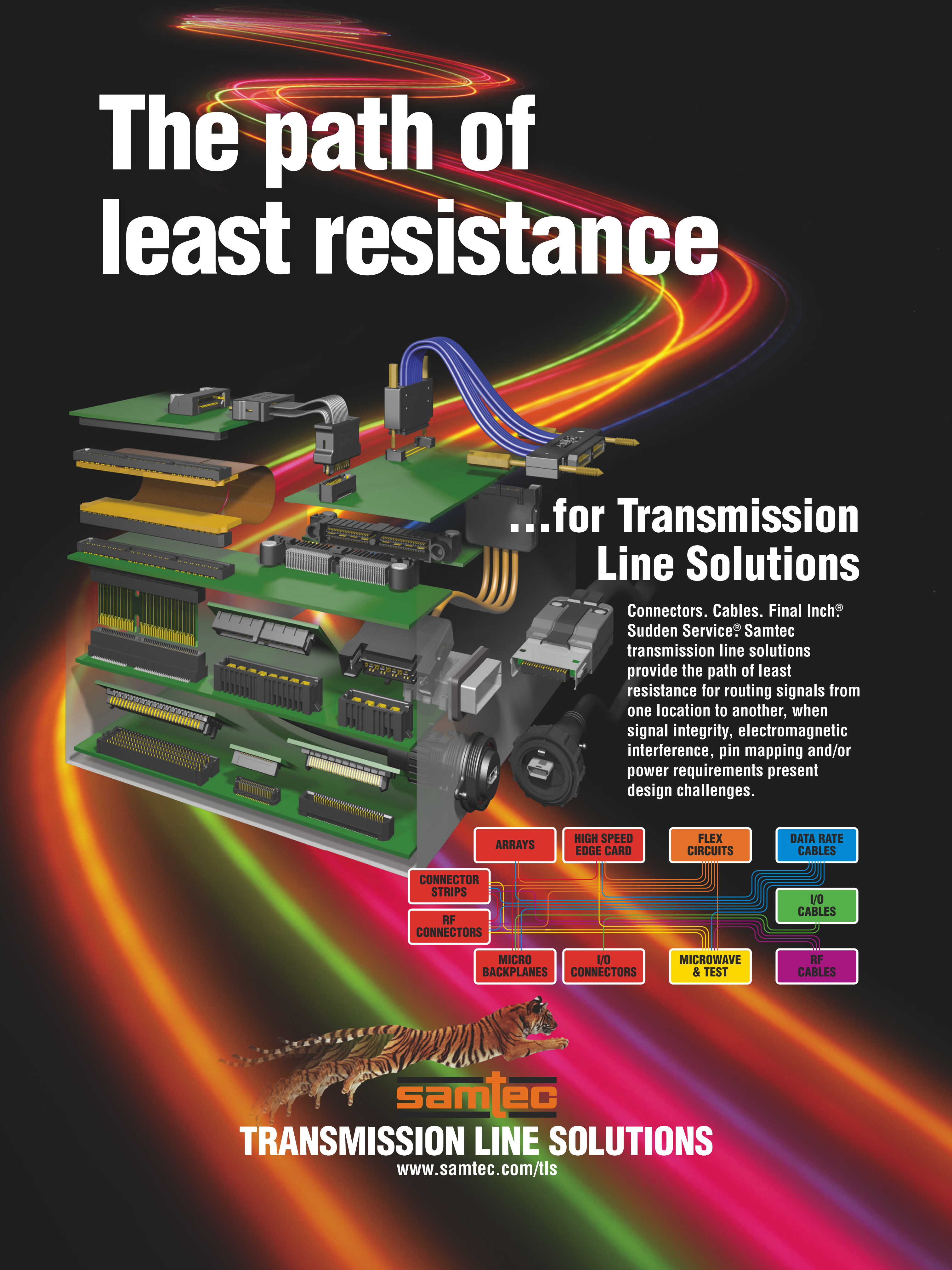
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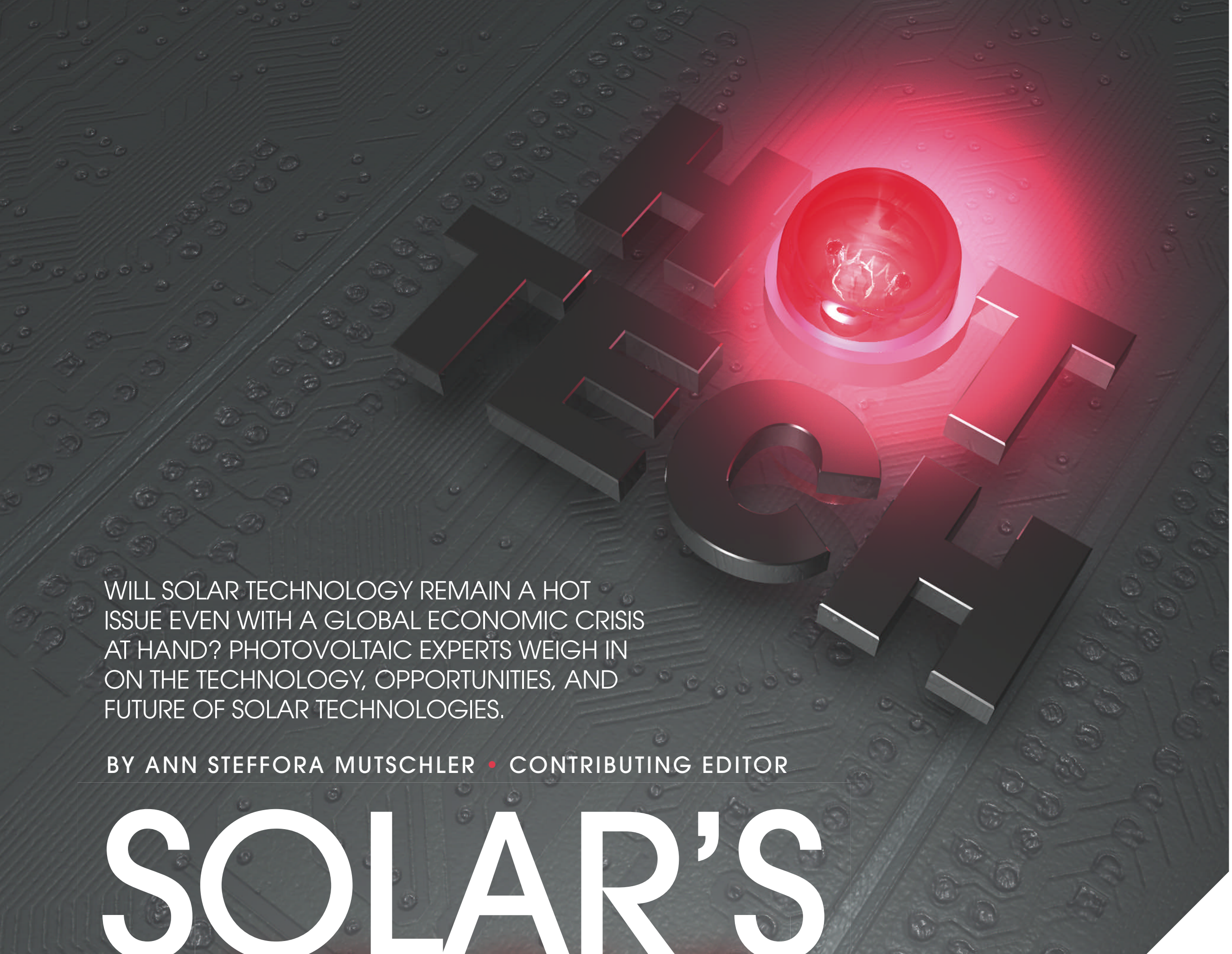

WILL SOLAR TECHNOLOGY REMAIN A HOT ISSUE EVEN WITH A GLOBAL ECONOMIC CRISIS AT HAND? PHOTOVOLTAIC EXPERTS WEIGH IN ON THE TECHNOLOGY, OPPORTUNITIES, AND FUTURE OF SOLAR TECHNOLOGIES.

BY ANN STEFFORA MUTSCHLER • CONTRIBUTING EDITOR

SOLAR'S BRIGHT FUTURE

Growing demand for clean energy sources, lower manufacturing costs, and more-advanced PV (photovoltaic) technology has in recent years driven the rapid expansion of solar-cell- and PV-array manufacturing. Even with a challenging global economy, industry experts say that PV technology will remain hot as the industry ramps up to meet growing ecologically savvy consumer and commercial demand for alternative-energy technologies, with growth rates already surpassing those of the semiconductor industry.

Just how big is the demand for solar power? Market-research company Gartner Inc reports that with the global market for electricity growing rapidly, there is significant growth on the horizon—from 17 PW (petawatt) hours in 2005 to a forecast 21 PW hours in 2010 and as many as 33 PW hours in 2030. From 2005 to 2010 alone, demand for electricity should increase 21%, outpacing population growth at 6%; 400-GW (gigawatt)-scale power plants, mainly based on fossil fuels and nuclear power, will meet this need.

If estimates hold up, by 2030, 2000-GW-scale power plants will be necessary to meet new electricity demand, and a potential need will arise to replace a large number of obsolete power plants. Demand on this scale, coupled with industrial and consumer demand and the desire to be free of foreign-fuel sources, has opened up significant opportunities for the PV market, Gartner says.

Some analysts believe that the solar-energy industry will be much larger than the semiconductor industry. "It could take 10, 15, or 20 years, but there's no doubt that it is so vital, so important, and so critical that this is a technology that is here to stay," says Alain S Harrus, a partner at Crosslink Capital and a 25-year semiconductor-industry veteran.

"With the financial crisis we've had in the [last few months], valuation of public companies has collapsed, and that [situation has] been reflected on the private side, as well," he notes. However, the economic slowdown has not stopped the amount of work going on in the PV industry and the number of new companies still trying to raise money. "A lot of these private companies have funding for … six, nine, [or] 12 months to two years, and, therefore, they just keep doing what they are doing because the market ultimately is there to make electricity at a cost competitive with fossil fuels," Harrus points out.

Paula Mints, principal analyst for Navigant Consulting's PV-services program and associate director of Navigant's energy practice, agrees that solar will continue to maintain the excitement it has garnered as of late. However, she says, the market is first going to soften, for the obvious reason: the economy. "People are drawing back on larger projects because credit is tight," she says.

Equal to that pressure, Mints says, is the cap Spain recently put on its feed-in tariff, a popular program in Europe. Given that Europe contains more than 70% of the global solar market, this blow was significant. "Spain has been growing enormously, a lot of product was shipped into Spain, and now it has nowhere to go," she notes.

As such, Mints is revising her solar-photovoltaics forecast downward for the next two years but still expects 25% growth for 2009, down from almost 60% growth in 2008, based on solar shipments of 5 GW to the first point of sale in 2008—not a bad growth rate compared with the semiconductor-industry figures.

Echoing Mints and Harrus, Jim Hines, research director for semiconductor and solar at Gartner, agrees that the outlook for the solar industry remains strong relative to other sectors of the economy. "This is an area where we expect to continue to see some pretty good growth rates," he says, a sentiment that October's Solar Power conference in San Diego reflected. "Talking to people on the show floor, there was a lot of optimism, and [the] outlook is strong for 2008 and 2009," he notes. Most module suppliers, especially the thin-film, PV suppliers, report strong demand.

Gartner expects crystalline-silicon-based PVs to remain the core of the market, reaching 13 GW sold by 2012, thanks to both the large installed base of manufacturers and the fact that the technology has a higher efficiency rate than its thin-film counterpart. It attracts users, such as residential installations and urban solar farms, with limited-footprint applications and a need for maximum electricity output.

Meanwhile, thin-film-PV technology imparts a strong opportunity with the potential to sell more than 4.5 GW by 2012, given its low-cost potential in overcoming the lower energy-conver-

AT A GLANCE

- Analysts expect a need for 2000-GW (gigawatt)-scale power plants by 2030.
- Wafer-based crystalline silicon has historically dominated the PV (photovoltaic) market and holds a 90% share.
- Most utilities see PV technology as experimental.
- Crystalline-silicon-based PVs attract users, such as residences and urban solar farms, with limited-space footprints and a need for maximum electricity output.

REACHING GRID PARITY

Perhaps the burning question in regard to solar power is when this form of energy will reach grid parity–with a cost equal to that of conventional, fossil fuel-based electricity.

Alain S Harrus (photo), a partner at Crosslink Capital, points out that there is not one answer that applies to the entire world. In California at 3 pm, a residential customer in a certain pricing "tier" is below grid parity–45 cents or more, whereas solar is at about 20 cents, he says. Comparatively, in the Pacific Northwest, where hydroelectric power generation is about 5 cents per kilowatt hour, solar doesn't make as much sense.

It is currently about three times more expensive to generate electricity with PV (photovoltaic) technology than with fossil fuels. But strong efforts to reduce costs in crystalline PV and thin-film PV could allow grid parity to occur between 2012 and 2015.

However, the grid-parity argument is invalid to some experts, including Andrew Skumanich, PhD, founder of SolarVision Consulting. Grid parity is an artificial notion, he warns.

"You're comparing solar panels to your wall plug for the toaster, and the problem is that, when you buy solar panels, you are buying hardware that is going to generate electricity," he says. "But you have to write a check for $20,000 or $30,000 for a typical house. … Even if you lower the cost to … maybe $15,000, you're still paying only 10 or 15 cents a kilowatt hour out of the plug."

Skumanich cautions against rationalizing that, over the life of the house, you're paying 10 cents per kilowatt hour, which is the same as the grid: "You can't lose sight of the fact that you said, 'over the life of the house.' That's pretty major. When you are writing the checks for the month, do you want to write a check for $15,000 for something that is not going to pay back for 10 or 15 years?"

sion efficiency for installations without space constraints, such as rural systems. A limiting factor to the growth rate of thin-film-PV technology is the time it takes to reach high-volume production and obtain product certification before utilities integrate the technology into their power mix, Gartner reports.

Hines also notes that the feed-in tariff cap in Spain has caused inventory to build up, also affecting price; the industry is addressing the problem, which doesn't appear to be long-term. On the other hand, market researchers at iSuppli Corp expect prices for polysilicon to create PV cells to drop in 2009 and the following years because of imbalances in the solar-supply chain (**Reference 1**).

RACE FOR EFFICIENCY

Wafer-based crystalline silicon, which comprises monocrystalline and polycrystalline, has historically dominated the PV market and holds a 90% market share. The remaining 10% of the PV market currently comprises thin-film-solar technology, including cadmium telluride, amorphous silicon, and copper indium gallium diselenide.

Cadmium telluride is currently leading in thin-film-PV applications because it is the only thin-film-PV technology in volume production. First Solar leads the way with its 0.5-GW manufacturing capability. The peak efficiency for cadmium telluride is 16.5%, with an average efficiency of 11%. There are also concerns about the recycling of toxic cadmium.

Silicon-based thin-film PV includes two fundamentally different cell structures, according to Gartner's Hines. One employs amorphous silicon, which has relatively low efficiencies of 6 to 7% and is the material most companies are starting with to ramp up production. The other silicon-based thin-film-PV technology is tandem junction, which combines amorphous silicon and a microcrystalline-silicon layer. Applied Materials and Oerlikon are the major vendors in this segment. Tandem junction is in the early stages of qualification but is not yet in high-volume production. Currently, its low efficiency rates restrict its use to installations with low land cost, limiting residential use, but make it a strong contender for solar farms. "When customers of Applied and Oerlikon are able to move that technology into production and begin manufacturing panels based on tandem junction, they expect to get efficiencies around 10%, which should be competitive with cadmium telluride," Hines says.

Copper-indium-gallium-diselenide-PV technology is a bit of a wild card, he points out, because it has demonstrated efficiencies as high as almost 20%, according to a study at the National Renewable Energy Laboratory. But lab tests differ from real-world tests. "The challenge with [the material] will be [determining whether it can] really deliver that level of efficiency in a production-worthy process on panels that are robust enough to survive a 25-year expected lifetime in the field," says Hines.

"It's going to be a race between the silicon-based and cadmium-telluride-based thin-film technologies to see which will get the lowest cost per watt. Clearly, First Solar has an advantage and a pretty substantial head start [with its] cadmium-telluride approach," he says.

Still, industry participants widely agree that there is room in the market for both thin-film- and crystalline-silicon-PV technologies to coexist and serve different market segments. "Crystalline silicon [can] deliver higher power densities, which is an advantage in installations where you're trying to maximize the power output from a given amount of area, [such as] a residential rooftop or even on some commercials rooftops," says Hines. "It really depends on how you are trying to maximize power output or minimize cost. For that reason, crystalline silicon will not go away. There is a lot of work being done to reduce cost on the crystalline side through using less silicon material and thinner wafers."

With thin-film technology, it's a somewhat different story, he asserts. "There's a lot of innovation going on, and it is really too early to pick the winners. First Solar has a very strong first-mover advantage with its technology, so it is really up to the new guys to deliver a compelling advantage that will enable them to take share away." Hines warns that a silicon-panel producer that can drive lower costs through better economies of scale or a copper-indium-gallium-diselenide design with significantly higher efficiency would disrupt the market.

SOLAR-GROWTH DRIVERS

From a technology point of view, the PV industry is moving along at a fast clip, but the size of the industry is actually a growth inhibitor. The fact that PV technology represents such a small part of global energy demand causes most utilities to look at it as an experimental program. Gartner estimates that total global-PV sales will reach almost 4 GW this year.

Cathy Boone, senior director of global marketing and government relations in Applied Materials' solar-business group, notes that, even though solar technology has been around for a while, manufacturers have never been able to produce it on a scale that would allow it to solve the world's energy problem. "Right now, solar produces 0.01% of all of the world's energy," she says. The international energy agencies say that, every year, we'll need to add about 120 to 130 GW of new generating capacity, with a gigawatt being enough power for San Francisco. So, add about 120 San Franciscos' worth a year."

According to Navigant's Mints, incentives are the only factors that drive

demand in solar unless it is off-grid. "The Spanish market is a case in point," she explains. "[Spain] put a cap on [its] market, and now the whole world shrinks because of that [decision]. These are really expensive programs that are very difficult to design. They have to be designed to stimulate a market [but] also be controllable and economically viable because someone has to pay for it. Essentially, where there are incentives, there will tend to be a market. This [situation] is a little offset right now because of the economy, but I don't think anyone believes the recession will go on forever. … Once there is a recovery, the proper incentives will be in place to drive demand."

Gartner's Hines agrees that government subsidies drive demand for this product. Therefore, growth depends on the ability of governments to support investments in solar projects through these subsidies in whatever form they take: feed-in tariffs, as in Germany and Spain, or other incentives that exist in the United States. It appears that the subsidies are intact for now, he says, but if the economic situation worsens or stays bad for a longer time, governments might have no choice but to pull them back.

Another concern of equal importance is the availability of financing for large solar projects. Even though interest rates are low, the tightening credit situation could affect those projects. In fact, Applied Materials confirmed in its fourth-quarter fiscal results in November that solar projects are seeing delays because customers are having difficulty getting funding (**Reference 2**).

But Applied officials remain optimistic. "We see a lot of opportunities in the solar market, and a couple of things drive that [opportunity]," says Boone. "First, government incentives still are quite strong for solar. The United States finally [passed] the extension of the ITC [incentive tax credit], and, for the first time, that tax credit is now available to residential homeowners without a cap—that means any size system." The $2000 cap limited who could take advantage of it, she explains. "And we certainly don't want to be in a position where … only people at a higher-income category can afford to get solar."

Second, Boone adds, Applied sees the ability of utility companies to take advantage of the ITC for the first time as a groundbreaking opportunity. "When we look into the future, we see a very clear divide in the solar market: the residential-rooftop and small commercial-space-constrained installation, dominated by the wafer-based crystalline-silicon products that are very high in efficiency but a little bit more costly. That is a market that we see growing in both the United States and Europe."

The company is also seeing the rise of what it believes is going to be the

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"transformative heart of solar's answer to the energy equation," as Boone explains, which is utility-scale solar. "Allowing utilities to capture tax credits for solar-generation facilities is going to unleash a lot of demand here in the United States. We have a lot of sun in the United States. Germany, the largest solar market in the world, gets as much sun as Maine, and that's not a very sunny place. We see growth in places like California, the Southwest, and the Southeast," she notes, pointing to Florida as an example. Last year the state passed a new RPS (renewable portfolio standard) that essentially is going to require its utilities to get a certain amount of generation from renewable portfolios.

SOLAR OPPORTUNITIES

Solar is set to continue to grow at a rate that many in the semiconductor industry have noticed, even with high residential costs and the arguments against "grid parity"—when solar's cost equals that of conventional electricity (see **sidebar** "Reaching grid parity"). Fortunately, semiconductor companies can play a part in the solar industry in power management, balance of inverters, microcontrollers, test systems, and automation.

The semiconductor industry has made a dent in solar, as Crosslink Capital's Harrus observes. "A good majority of the solar start-ups in Silicon Valley are staffed by semiconductor people—on the process side, on the equipment side, on the management side—and the core technology comes out of universities or national laboratories. There are dozens of examples of this [trend]." He believes people are realizing that the semiconductor industry is not what it used to be and are moving to the solar side.

Semiconductor companies that have made inroads in the solar market include Applied Materials, National Semiconductor, Linear Technology, and Analog Devices. Also, OEMs, such as Advanced Energy, have adapted their technology to fit solar factories. And, because part of solar installation is the power management, Advanced Energy, Analog Devices, and National Semiconductor are fitting in well; power control and power management are jobs the semiconductor industry knows how to do.

Gartner's Hines points out that there is more synergy between FPD (flat-panel-display) manufacturing and thin-film-solar-panel manufacturing than between the traditional semiconductor market and solar. Sharp, for example, one of the largest FPD manufacturers, is also the No. 2 solar-cell manufacturer, after Q-Cells, and just announced a major thrust into thin-film-PV technology. Hines believes there will be similar moves to come, citing Samsung and LG as examples.

POWER CONTROL AND POWER MANAGEMENT ARE JOBS THE SEMICONDUCTOR INDUSTRY KNOWS HOW TO DO.

In addition to opportunities for device makers, Hines notes, there is room in the solar market for some—but not all—semiconductor-manufacturing equipment and technologies. "Just because solar is silicon-based does not mean it represents an opportunity for every equipment company," he says. "If you look at the crystalline-silicon-PV-manufacturing flow, there are diffusion furnaces, deposition of nanoreflective coatings, [and other factors]. And, while there are some similarities, there are far fewer processing steps, and there is really no need for advanced lithography. The metallization is far less critical. They are using screen printing and silver paste." Still, he notes, as the industry evolves, there is a great opportunity to learn from the semiconductor industry about how to improve the manufacturing efficiencies within the PV market. He suggests looking at opportunities in process control, metrology, inspection, and automation technology.

On the thin-film side, the big crossover is from FPD manufacturing. Applied Materials and Oerlikon are leveraging capabilities that they developed in this area.

On the downside, the transition from semiconductor to solar is not always sunny. Although solar and semiconductors are fundamentally about silicon and technology, the similarities end there, says Andrew Skumanich, PhD, founder of SolarVision Consulting. For chips and semiconductors, "You're trying to build more and more complexity in and make it more and more functional," he says. "You can charge for that." With solar, "Absolutely everything is about lowering the cost and not necessarily increasing the complexity," he says. "What you talk about is a metric: dollars per watt." It may be difficult for a semiconductor company to adjust its focus from improving functions to reducing costs and improving productivity.

SUCCEEDING IN SOLAR

A semiconductor company can theoretically make the transition to becoming a successful player in the solar industry, Skumanich says. "But if [it goes in thinking], 'Well, we've got hotshots in technology, and what's solar but another way of making a diode?' then, [it's] going to have problems, because, … even though [the company] might have a good approach, it doesn't make the overall cost go down, and it won't fit into the market," he cautions.

Crosslink's Harrus points out that, to achieve success in the solar industry, "the technology is less than 25% important; 80% is excellence in low-cost manufacturing because electricity is a commodity."

"When we're making chips—with the exception of memory, which is a commodity—there is a whole value chain, and you're pricing to value. You can have great gross margins on chips that are valuable, but electricity is a commodity. We don't care when we throw the switch on where the electrons come from; we want to pay the least possible amount," he says, noting that the solar market differs from the conventional chip industry, in which the quality of your phone, for example, depends on the quality of the chips inside.

"We are at the stage where technology sometimes is very interesting, but nobody cares," says Harrus. People understand that, if you can't manufacture something in high volume, it is a waste of time. EDN

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AUTHOR'S BIOGRAPHY

Contributing Editor Ann Steffora Mutschler was most recently a senior editor for EDN. In that position, she wrote daily news, feature articles, and "The Sandbox" blog, keeping her finger on the pulse of the leading chip providers as well as the design-and-manufacturing-tool providers. In addition to her engagements at EDN, Mutschler has more than 10 years of editor experience in the industry, including stints as managing editor for EDACafe.com and EDAVision, as well as public-relations work. Currently, she is working on a number of freelance writing projects.

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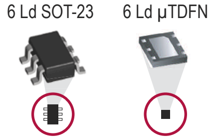

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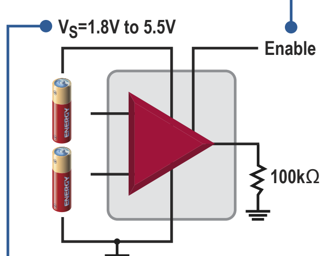

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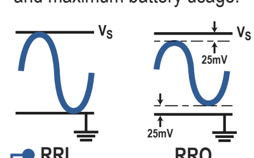

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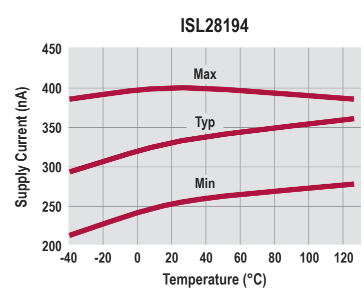

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BY JON M QUIGLEY, VOLVO 3P • KIM H PRIES, STONERIDGE ELECTRONICS

Automotive embedded development and testing

AUTOMOTIVE-EMBEDDED-SYSTEM DESIGNERS FOLLOW INDUSTRY-STANDARD GUIDELINES TO GUARANTEE PRODUCT QUALITY AND ADDRESS PRODUCTION IMPLICATIONS.

The automotive world, which includes commercial and personal vehicles, developed its own approach to product and process development. Embedded-system developers who work in this environment use a different set of tools and answer to a different set of expectations from those of, for example, developers in the medical or aircraft industries.

The automotive industry uses as its principal framework for development and production APQP (advanced-product-quality planning), which the AIAG (Automotive Industry Action Group) defines. The phases are typically, but not exclusively, conceptualization, product design and development, process design and development, and product and process validation.

The APQP approach is a high-level "waterfall" model. At no point are there any restrictions that would prohibit spiral or agile approaches to software development. The manual does specify a minimum number of deliverable documents and activities. It does not specify a limit to the amount of documentation, although the formality of the PPAP (production-part-approval process) requires a submission—in full form—of at least 18 and often many more documents.

The higher-level automotive-quality standard, ISO (International Organization for Standardization)/TS 16949:2002, is a superset of the ISO 9001 quality-system standard with an automotive spin. It does not explicitly prescribe APQP, but APQP aptly meets the requirements of the standard.

REFINING THE APPROACH

During the concept phase, the development team defines and plans the development program. This phase of APQP probably has the largest quantity of soft deliverables. Initially, the embedded-development team solicits the voice of the customer in an appropriate format. Some organizations may use quality-function deployment, whereas others may use proprietary approaches to capturing customer desires and needs. In many ways, this phase is the most crucial because incompetence during the opening game will almost certainly result in failure in the end game. In no way should the development team override the voice of the customer with the voice of engineer unless a safety issue is involved; the team can, however, make recommendations.

The APQP framework recommends that the team secure benchmark data. Getting this information from competitors is problematic at best and unethical at worst. However, it may be possible to research the trade journals and similar work at noncompetitors and put together enough information to set performance targets. Additionally, the development team can use internally generated data for the same reasons. Performance targets will allow the team some modicum of reality when estimating schedules and milestones.

By the end of this phase, the development team will have

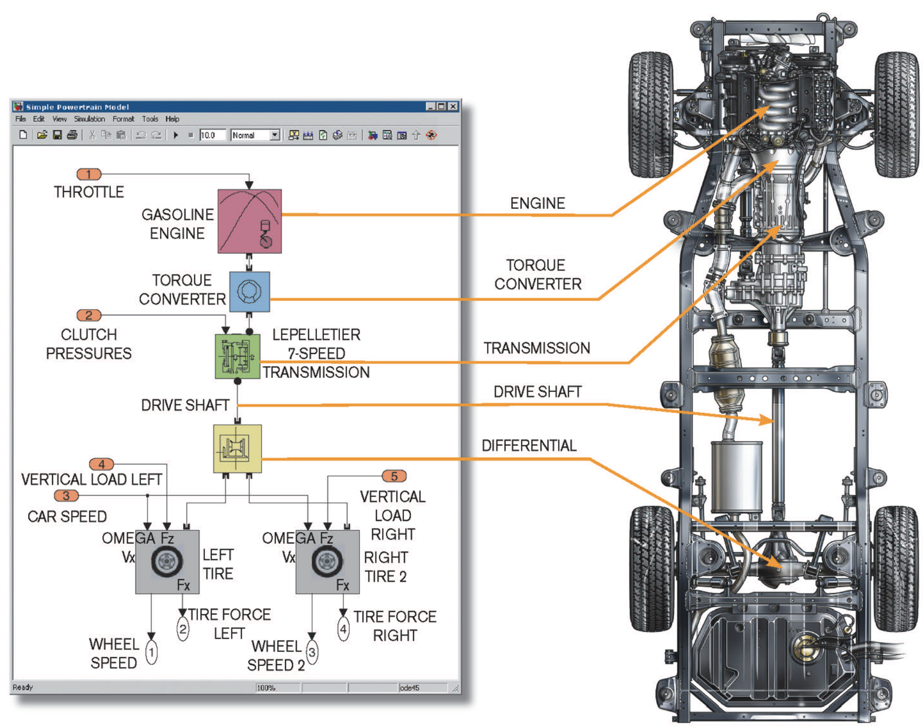

Figure 1 SimDriveline extends The MathWorks' Simulink with tools for modeling and simulating the mechanics of automotive-drive-train systems.

defined design, quality, and reliability goals; will have developed some idea of the hardware platform; and will have secured formal management support. In short, the team will march into product and process development with a firm footing in reality and a clear understanding of where it is going.

The software-development team should produce a catalog of desirable and undesirable behaviors in the form of a software-requirements specification. The software-specification document, which can be a FAST (function-analysis-system-technique) diagram, is in many ways more important than software-design documentation. The test group and the designers measure the performance of the software against the requirements rather than the design.

APQP organizations tend to develop both products and processes simultaneously or nearly simultaneously. Sometimes, the process design and development starts after the product design and development commences; otherwise, they run in parallel.

The enterprise can manage product design and development using whatever development model it favors. However, the automotive approach has some unique elements. Some organizations prefer a requisite amount of design documentation; however, any well-qualified software engineer recognizes that the code itself is the most up-to-date instantiation of the design. In general, the difficulty with design documentation lies with the divergence between code and documentation almost immediately after the engineers begin writing the actual code.

One of the most powerful tools in the automotive approach is the DFMEA (design-failure-modes-and-effects analysis). Using DFMEA, cross-disciplinary teams of development engineers analyze the functions of the product using a logical approach—for example, FAST—and develop a table that captures failure modes, causes, effects, and qualitative values related to these events. The tool works best when the teams use it to solve design issues. The embedded-software-development team can also use the DFMEA with some forethought: Software becomes complicated exponentially, leading to astronomical requirements for test cases. The DFMEA is a design tool for upfront thought on potential problems, so it is still valid for the software engineers to use.

The embedded-software-development team will also need to consider design verification. The automotive world uses a summary document called a DVP&R (design-verification plan and report) to capture all of the activities that verify whether the design meets or exceeds requirements. The team should derive the activities in the DVP&R from the DFMEA, which has a detection column for this purpose. A minimal design-verification plan should include verification that the software meets customer baseline requirements; stimulation of every input to the firmware using combinatorial approaches, including pairwise testing, three-wise testing, designed experiment arrays, and extreme product-destroying tests; and stochastic testing to present the software with unexpected conditions.

Furthermore, it is common to acquire actual vehicle components, including wire harnesses, to be able to test the software with hardware-in-the-loop simulation. The improved verisimilitude increases confidence that the results are relevant to the final product.

The development team should not ignore the possibility of using one or more software-based simulators to provide the appropriate signals or messages across one or more buses. The team could even use older products with specially developed software to simulate brake controllers, engine-control modules, transmission controls, and other devices in modern vehicles. Other approaches include the use of commercial products, such as The MathWorks' (www.mathworks.com) Matlab/Simulink (**Figure 1**), National Instruments' (www.ni.com) LabView, and other tools that can communicate directly with data buses, analog-to-digital controllers, digital-to-analog controllers, digital-to-digital controllers, and various serial and parallel ports.

If the software team is fortunate, it may be able to test its work with prototype designs using ICEs (in-circuit-emulators), which allow for hardware, software, and interaction assessment during verification. The use of prototypes is highly desirable but can be expensive. Simulation will allow for some level of testing before a prototype becomes available.

IV&V (independent verification and

validation) brings a level of honesty to the testing process. It is not so much that the development is dishonest but rather that the developers understand too well how their software works. An IV&V group develops its own understanding of customer requirements and builds its own test-specification documents. Alternatively, the enterprise may prefer to have a third-party organization provide this function.

The automotive-product-design process requires design reviews; however, the manuscript does not prescribe the frequency of these reviews. Experience suggests that relatively frequent, short reviews add more value and reduce risk better than do infrequent, long reviews. The individual enterprise may have a launch process that specifies the exact number of formal reviews. The software team can always implement more product reviews than the launch process specifies.

Because the embedded software will reside on the product as firmware, the development team must consider how to implement its software on the product and, further, how it will coordinate software activities with the manufacturing process.

During this quasiparallel phase, the team decides how to program the microcontroller and how and when to release the software to production. It also coordinates with the automated-test-equipment group to make sure the expected and unexpected behavior of the product is well-understood. The software-development team can also make life easier for the manufacturing people by adding, for example, built-in self-testing, which simplifies life for the automated-test-equipment group; self-calibration features if the product has gauges or some other device that provides visual indications of a measurement; and boot-loading capability, so the team can "reflash" the product if the hardware has flash memory.

Product validation is not equal to design verification, although, in practice, the test suites are often similar. The purpose of product-validation testing is to assess whether the product meets engineering standards the teams set during the product-and-process-development phases. Because validation normally occurs during the end game, the developer should no longer be performing design verification.

Process validation is decidedly different from product validation. The expectation is that you use the final process, the production-ready materials, and the launch software release and that a PCP (process-control-plan) automotive document describes all other activities. The PCP details how the manufacturer will fabricate the product—from measurement values to reaction plans to process capability, an index of quality.

CORRECTIVE ACTION

The APQP shows corrective action occurring throughout the development and launch, which makes sense; issues requiring formal correction occur from the start of the project, up to launch, and sometimes afterward. In the automotive world, developers frequently document corrective action using the 8D (eight-disciplines) model.

The 8D model is a rational approach that provides steps such as emergency action, containment action, and irreversible corrective action. An emergency action involves stopping the manufacturing line if, for example, the verification team or the software team determines that the software has a safety issue. A containment action occurs when you can detect the problem and sort out the bad units. For example, when you have captured a marginal hardware design and weak firmware, some of the components may still be good enough to ship if you properly test the unit. Irreversible corrective action

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occurs after deep probing to find what is usually called root cause. Eliminating the root cause eliminates the problem. Sometimes, containment is the best you can do. Each action has a verification component to ensure compliance.

The embedded-development team can use all of the 8D components as a means of formally documenting corrections. The key idea with this approach is the elimination of the problem's cause.

The feedback component of APQP involves the assessment of customers' reactions to the product, measurement of issues that arise, product and process changes, and lessons learned during development and launch. The APQP process allows learning to occur naturally, and capturing errors and potential errors becomes a way of building a culture of prevention.

Other components of the feedback system are risk assessment and mitigation. Experience suggests that compressed schedules will lead to software errors and that customer dissatisfaction will follow. One approach that incorporates feedback as well as risk management is the TEMP (test-and-evaluation-master-plan) technique, which the US Department of Defense employs. In this approach, the customer and developers agree ahead of time to deliver a sequence of software packages. Each new software package is a superset of the previous package, and each package is fully functional. This method helps restrict the errors to the new software and simplifies the testing activity, because the test function will need to run a regression suite only on the previous software package to verify that no detrimental interactions occurred during development. If this approach sounds to you like a precursor to agile-software development, you're right.

RELEVANCE ELSEWHERE

The PCP approach is suitable for any sequence of steps in a process and provides a framework for documenting requirements, particularly those involving measurement. It is similar in concept to the HACCP (hazard-analysis-and-critical-control-point) process-flow documentation that the food industry uses. You can also use the PCP to document a software-development process. The development team would then apply a PFMEA (process-failure-modes-and-effect analysis) to assess the need for added controls on the process.

Both design and process FMEA tools aim to eliminate product and process problems before they occur. Prevention is generally cheaper than detection and correction, not to mention the wasted time that prevention eliminates.

The reviews, the production-part-approval process, and all the other automotive documents help the development teams assess their work so they can release a product they can be proud of. In general, some process is better than no process. The APQP framework provides a general process without being heavily prescriptive when it comes to software development—allowing automotive companies the flexibility to evolve systems that suit their needs and still fitting within the overall model. Use of the APQP model for development also has the benefit of providing a common vocabulary and similar metrics and expectations from one enterprise to another. **EDN**

AUTHORS' BIOGRAPHIES

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Kim H Pries is director of product integrity and reliability/quality-management systems at Stoneridge Electronics—North America. Current responsibilities include all test-and-evaluation activities, including laboratory, calibration, hardware-in-the-loop software testing, and automated test equipment. Pries holds bachelor's degrees in history and metallurgical engineering from the University of Texas—El Paso plus a master's degree in metallurgical engineering and materials science from Carnegie-Mellon University (Pittsburgh).

Program “excelerates” microcomputer-I/O allocation

Aubrey Kagan, Emphatec, Markham, ON, Canada

When I designed a system employing the LPC2138 ARM (www.arm.com)-based microcontroller, I quickly abandoned a pencil-and-paper approach to allocating the I/O. That method is tedious and error-prone because of the large number of pins on the microcontroller. Instead, I entered the data into Microsoft (www.microsoft.com) Excel (**Reference 1**). This approach let me assess the initial amount of I/O and any additional I/O that I would have to add. With the spreadsheet, I could create a rough bill of materials for a quote. Thereafter, it helped with the functional allocation and is an elegant and practical approach for almost any project. The online version of this article, at www.edn.com/081215dia, provides a sample spreadsheet that you can download.

First, you enter all the pins in ascending order (Column A in **Figure 1**). The LPC2138 can have as many as four functions per pin. Columns C to F show the functions and their corresponding pin numbers. Next, you insert the data-validation feature in each concomitant cell in Column B. When you click on a cell with this setup, a drop-down arrow appears, and a selection of the cells appears to the arrow’s right. You click on any cell in Column B and then click on the “data” menu and then the “validation” menu to see the setup of data validation. You format cells for which no options are available, such as V_{SS}, with a black background because, at start-up, you can delete the whole column to initialize, but the color formatting will remain.

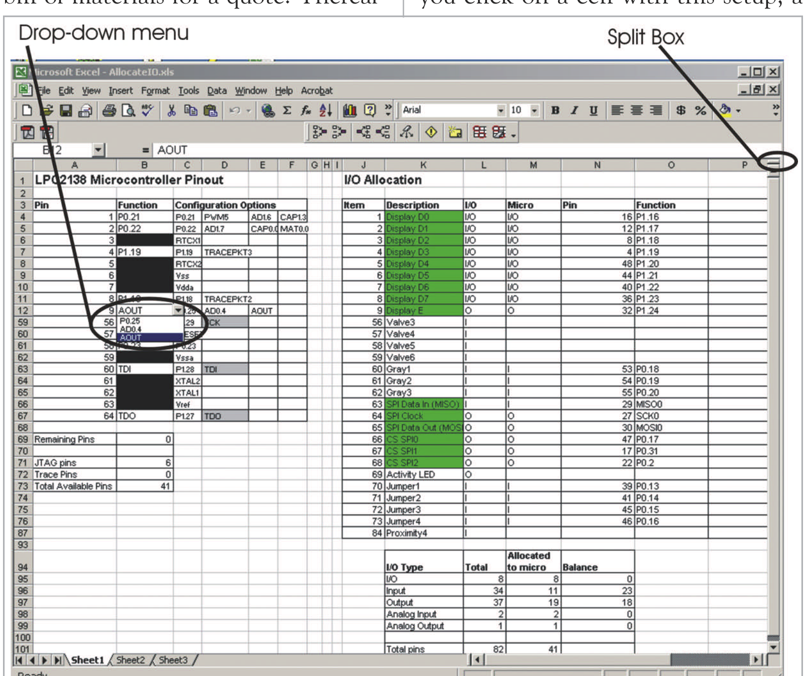

Figure 1 The completed worksheet has a large number of hidden rows to show the top and the bottom of the range.

You enter the project’s I/O in the I/O-allocation table (columns J to O). You classify each pin as I (input), O (output), I/O (input/output), AI (analog input), or AO (analog output). You must allocate those pins to the microcontroller. Any I/O device that is not green is a direct user decision and not a function of anything else on the worksheet. Note that the information that appears in the pin column (Column N) is not the pin number but a reference to the pin number in Column A, so that, if you were allocating the function to Pin 8, the entry is “=A11,” as it is in Cell N6. Column 12 contains a look-up formula that fetches the function name that appears in Column B to the right of the selected pin.

The bottom of each table (cells A69 to B73 and K94 to N101) includes

DIs Inside

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some statistics on the usage and availability of pins based on the allocation to allow you to keep tabs on the allocation as it progresses. Cell M101 has conditional formatting, so it turns red if the pins you allocate to the microcontroller exceed the total number of pins available on the microcontroller as calculated in cell B73. You can add hardware I/O to the right of the table to ensure that you include all I/O.

The usage of the spreadsheet takes place as follows:

1. Delete cells B4 to B67.
2. Delete cells K4 to N87.
3. Create a list of project I/Os and fill in the I/O-allocation table. Insert rows for additional pins, remembering to update the entries in columns K and O.
4. Allocate those pins on the microcontroller that you cannot use for general I/O, such as the JTAG pins for emulation.
5. Drag down the split-box indicator so that the worksheet appears something like that in **Figure 2**.
6. In the upper pane, select the cell in Column B associated with the desired pin. Select the configuration from the drop-down box.
7. Go to the project-I/O function in Column N in the lower pane. Enter an equals sign and then click on the desired pin in Column A in the upper pane, scrolling up or down if necessary. The selected cell reference then fills into the formula. Complete the entry with the "enter" key.
8. Repeat for all the I/O.
9. Drag the split-box indicator back to the top to remove the screen split.

Some of the features in Excel can really make this model shine. For instance, the pin allocation of the LPC2138 does not follow the logical ordering of the pins. Perhaps it would help to see Port 0 listed in ascending order. You can use Excel's sort feature to group like functions together.

To see where the information comes from, click on any entry in Column N, select the "tools" menu item, then select "auditing" and "trace precedents." If you use this procedure with all the cells, you can visually trace unallocated or twice-allocated pins. A macro, "find all precedents," which is available in the Web version of this Design Idea at www.edn.com/081215dia, results in the screen in **Figure 3**. Another macro, "clear arrows," also available on the Web site, clears all these indicators. Unfortunately, because the look-up table in Column O includes a reference to Column A, you cannot use the antecedents' trace in the same manner. **EDN**

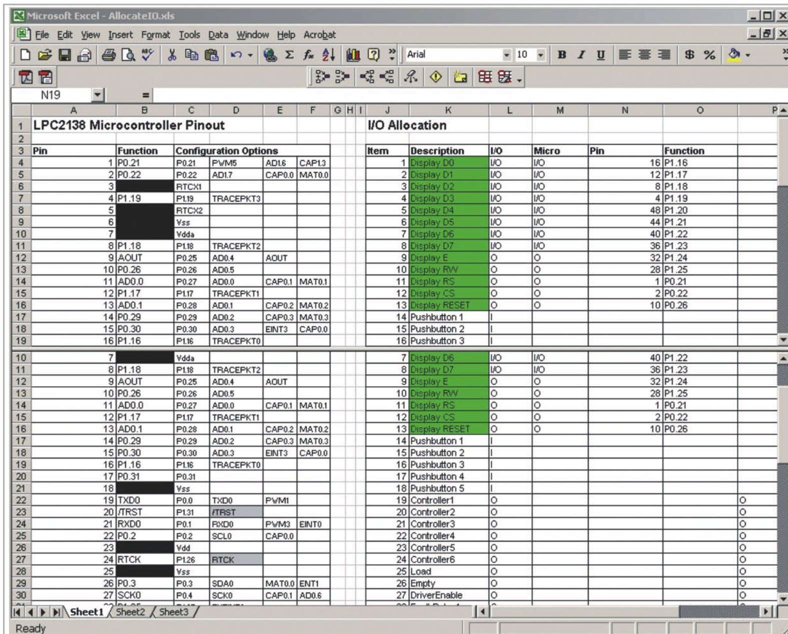

Figure 2 Two panes with the split box allow for easy pin allocation.

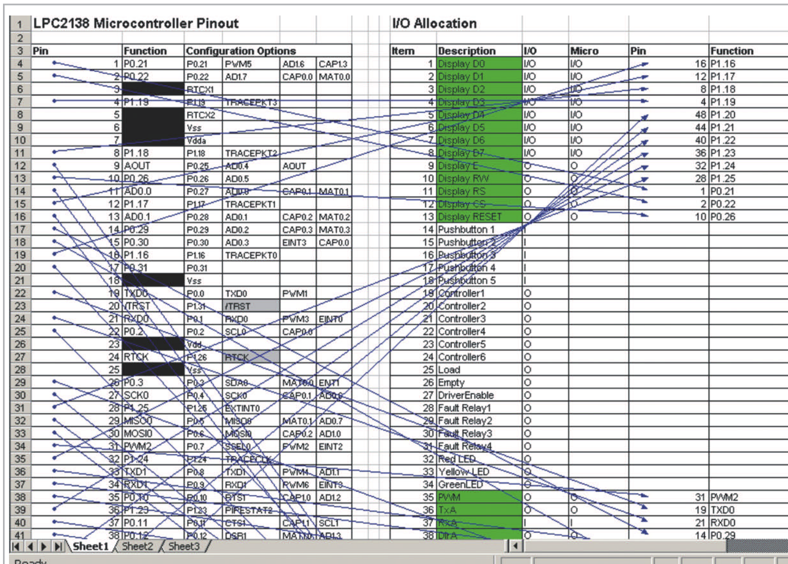

Figure 3 The precedent feature lets you verify that you have allocated all the pins and that each pin has a unique assignment.

REFERENCE

1 Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Elsevier/Newnes, May 2004, ISBN: 0750677562.

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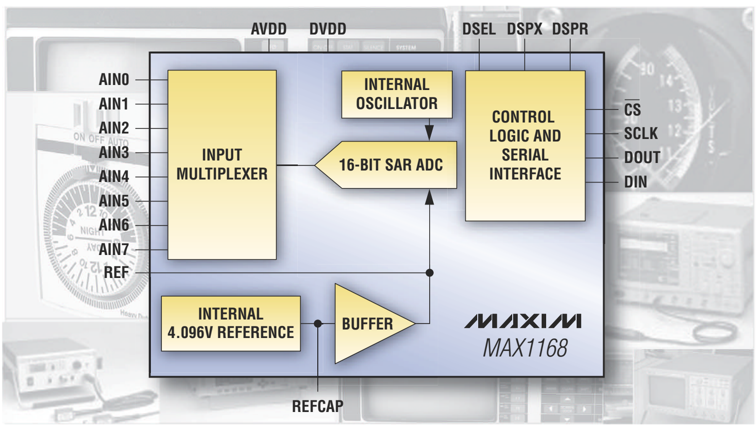

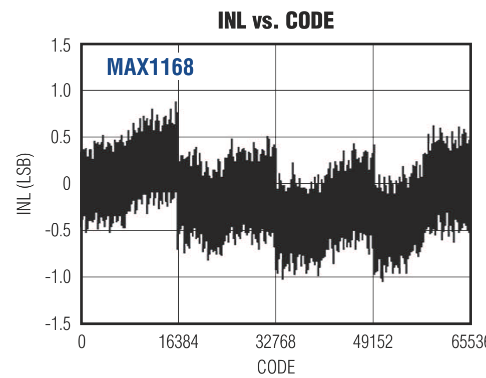

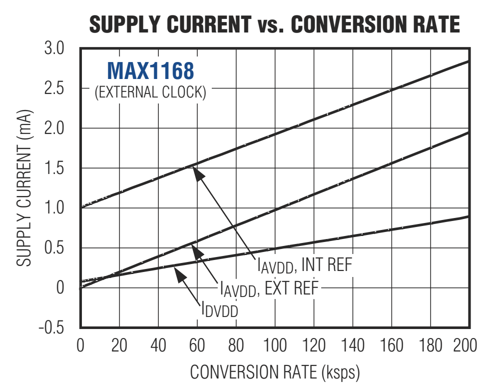

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Part	Resolution (Bits)	INL (LSB)	DNL (LSB)	Speed (ksps)	Channels	Supply Voltage (V)	Package
MAX1168	16	±1	±1	200	8	5	24-QSOP
MAX1167	16	±1			4		16-QSOP
MAX1068	14	±0.5			8		24-QSOP
MAX1067	14	±0.5			4		16-QSOP

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Microcontroller measures resistance without an ADC

Ashish Aggarwal, Netaji Subash Institute of Technology, Dwarka, India

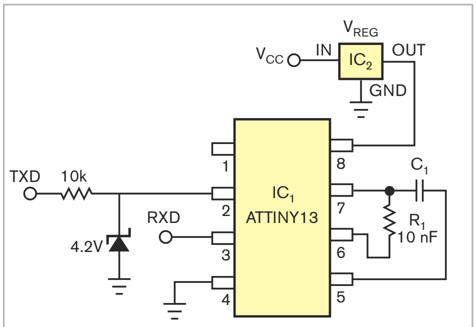

Figure 1 This circuit can measure resistance by measuring the frequency of a microcontroller configured as an astable multivibrator.

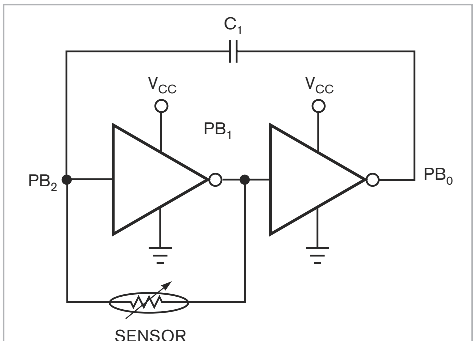

Figure 2 This design implements an equivalent oscillator based on the principle of an astable multivibrator in the Tiny13.

Sensors automate most of the processes in industry. Most of these sensors, such as those for ammonia gas, temperature, and the like, are resistive devices in which electrical resistance changes—mostly nonlinearly—as the surrounding conditions change. The sensors' resistances may vary from 1 mΩ to 10 MΩ. **Figure 1** illustrates a circuit for resistance measurement. The circuit uses an eight-pin AVR microcontroller, a Tiny13V from Atmel (www.atmel.com), for the controller. The Tiny13V works over a supply-voltage range of 1.8 to 5.5V.

This design implements an equivalent oscillator based on the principle of an astable multivibrator in the Tiny13 (**Figure 2**). The oscillator has no stable states, and the signal keeps oscillating between two quasistable states. This oscillator produces a frequency that depends on the value of the resistor. As resistance increases, frequency decreases, and you can easily measure this frequency to yield the value of the resistance.

The resistance you want to measure connects between any two general-purpose I/O pins of the microcontroller, and a capacitor, C_1, of known value connects across the other general-purpose I/O pin. Note that PB_0 and PB_1 are always in different states to implement a NOT gate. PB_2 measures a high or a low across resistor R_1.

Initially, PB_0 is high, PB_1 is low, and there is a high-impedance state at PB_2. As a result, the capacitor starts charging with time-constant RC. Note that the capacitor initially acts as a short, and PB_2 senses a high. As the capacitor charges, the voltage across the resistor decreases, and, when PB_2 detects a low, PB_1 goes high and PB_0 goes low.

Next, as the capacitor discharges, the potential across the resistor builds up, and, when PB_2 detects a high, PB_0 goes high and PB_1 goes low. In this fashion, measuring the frequency or half the number of toggles of PB_0 in a second gives an inverse relation of resistance, R_1 (in **Figure 1**), with frequency, f: $R_1=k/f$, where k is a proportionality constant. The result travels to a PC through a serial RS-232 interface. Because the Tiny13 has no UART, a software UART program and the program for measuring resistance are available with the Web version of this Design Idea at www.edn.com/081215dib. **EDN**

Five- to 10-LED flashlight circuit runs at 3V

GY Xu, XuMicro, Houston, TX

Almost all inexpensive commercial LED flashlights use a 4.5V power supply—three AA or AAA batteries—because white LEDs require 3.3 to 3.5V to fully turn on. Thus, there is a voltage gap between LEDs and traditional 3V incandescent-flashlight bulbs. The voltage difference makes for a difficult—but not impossible—transition from the old flashlight to an LED flashlight. The simple circuit in **Figure 1** solves this problem.

The circuit is just a typical voltage booster comprising six components that you can mount on a small PCB (printed-circuit board) measuring less than 1 in^2. Component selection and their values are, however, important. IC_1, an Atmel (www.atmel.com) ATtiny13 microcontroller, works as a charge pump for boost control. Its internal oscillator frequency is 1.2 MHz at 3.5V, and it can operate with voltages as low as 1.8V with low power consumption. The ATtiny13 has a small, eight-pin footprint.

Q_1 is a low-saturation-voltage ZTX618 NPN transistor that can handle more than 3A of collector current. D_1 is a Schottky diode with low forward-voltage drop to achieve high efficiency. When you apply the 3V supply-voltage power to IC_1, IC_1 outputs a high pulse that turns on Q_1. Its collector is effectively grounded. Inductor L_1 charges linearly from 0A to some peak current until IC_1 outputs a logic low, and Q_1 then turns off (**Figure 2**). This circuit works only when the inductor is not saturated, so choosing the right inductor is important. At that mo-

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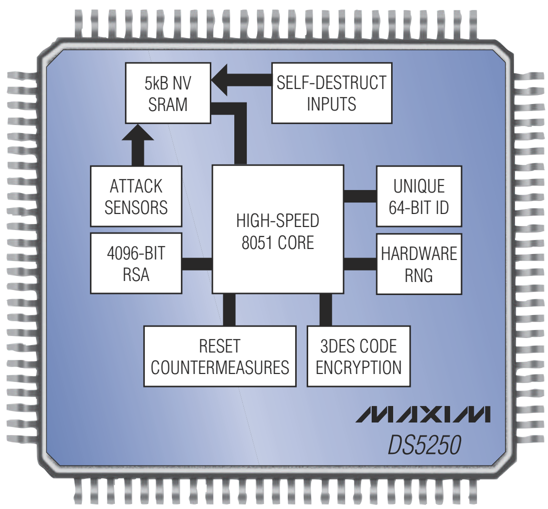

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Part	Temperature (°C)	Package
DS5250F+125	0 to +75	100-MQFP
DS5250F+825	0 to +75	80-MQFP
DS5250F+1N5	-40 to +85	100-MQFP
DS5250F+8N5	-40 to +85	80-MQFP

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ment, the established magnetic field in L_1 collapses, causing a reverse induced voltage that makes D_1 conduct. The energy in L_1 transfers to C_2, which stores the energy until it is sufficient to light up the LEDs. The relationship between the supply voltage (V_{IN}), the inductor (L), its peak current (I_{PK}), and the microcontroller's on time (T_{ON}) is $V_{IN}=L \times I_{PK}/T_{ON}$.

For a supply voltage of 3V, you should select an inductor with a nominal value of 10 µH and a saturation current larger than 1.5A. You can calculate the microcontroller's on time as 5 µsec. **Listing 1**, which is available in the Web version of this Design Idea, at www.edn.com/081215dic, uses this value for the charge pump's on time. The program in **Listing 1** is so simple that it takes only 22 bytes of the 1-kbyte program memory. The charge-pump-control function is easy to understand. The instruction Sbi portb, 2 tells the microcontroller to output a logic high to turn on the charge pump. Because the microcontroller works at 1.2 MHz by its internal oscillator, each NOP (nonoperation) takes one clock cycle, or 0.83 µsec, to execute, so the on time is 5 µsec. Similarly, Cbi portb, 2 tells the microcontroller to output a logic low that turns off the charge pump.

Measurement shows that the circuit works at a 100-kHz switching frequency and that the actual output is 17V/35 mA for five LEDs and 32V/20 mA for 10 LEDs. Unlike the usual voltage-booster circuit, this circuit needs no resistor, which wastes energy and generates useless heat, as a voltage divider or a sensor.EDN

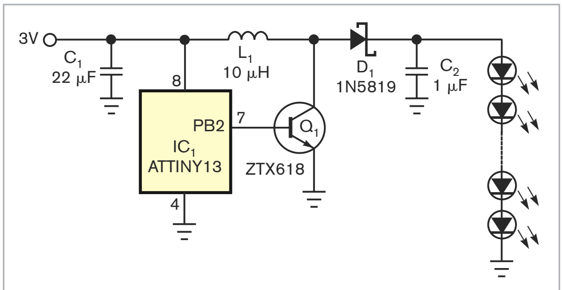

Figure 1 A charge-pump circuit creates the boosted voltage to light LEDs for a flashlight.

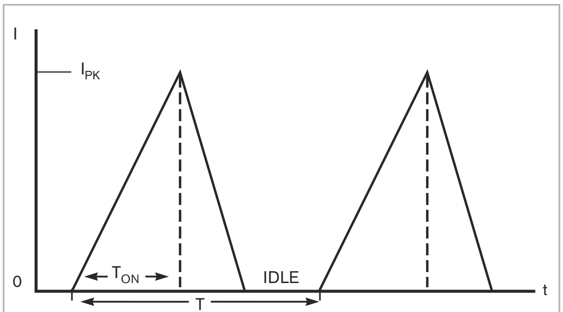

Figure 2 During the on time, current flows through the inductor and then charges the capacitor.

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CIRCUIT PROTECTION

Lithium-ion protector provides cell balancing for five- to 10-cell battery packs

The DS2726 stand-alone lithium-ion protection IC uses integrated cell balancing, suiting power tools, e-bikes, portable household appliances, battery-backup systems, or any applications using a five- to 10-cell lithium-ion battery pack. Features include overvoltage, undervoltage, discharge-current, and short-circuit protection. The IC allows configuration with no external microcontroller and provides protection by integrating cell balancing with fault-monitoring, high-side P-channel FET drivers. High-side protection allows the host systems to maintain communication with a

fuel gauge, even when a fault condition causes the protection FETs to switch off. Available in a 7×7-mm TQFN-32 package, the DS2726 stand-alone protection IC costs $4.58 (1000).
Maxim Integrated Products, www.maxim-ic.com

Protection ICs use high-accuracy voltage-detection circuits

Targeting lithium-ion/lithium-polymer rechargeable batteries, the S-8209A/B protection-IC series features a high-accuracy voltage-detection circuit and a delay circuit. A transmission function and two types of cell-balance function allow for the configuration of a protection circuit with multicell series. The ICs provide a 3.9 to 4.4V overcharge-detection voltage at a 5-mV step with a ±25-mV accuracy and a 7-mA maximum low-current consumption. An external capacitor for the output pin enables a settable delay time. Available in SNT-8A and TSSOP-8 packages, the S-8209 protection ICs cost 70 cents (10,000).
Seiko Instruments, **www.sii-ic.com**

Miniature ESD diode suits portable consumer electronics

The ESD0402-01FR TVS diode provides contact discharge protection suiting portable consumer electronics at 8-kV levels. Suiting use in a ±5V environment, the back-to-back diodes provide for bidirectional ac signals. The device allows dissipation of ESD strikes at ±8-kV contact discharge, according to the IEC61000-4-2 international standard. Available in a miniature DFN-2 lead package in 0402 case sizes or measuring 1×0.6×0.5 mm, the ESD0402-01FR ESD diode costs 3.5 cents.
OnChip Devices, www.onchip.com

ESD-protection device aims at fast data lines

Targeting high-speed interfaces, such as HDMI 1.3 ports, the IP-4281CZ10 ESD-protection device suits consumer electronics, including televisions, notebook computers, set-top box-

productroundup

CIRCUIT PROTECTION

es, gaming consoles, and DVD players. The device delivers 8 kV of contact-ESD protection, in accordance with IEC6100-4-2 standard Level 4 certification. An additional feature ensures that all pads are matched to 0.5-mm-traced high-speed lines, such as TMDS (HDMI) and ML (DisplayPort). Available in a 1×2.5×0.5-mm ultrathin leadless package, the IP-4281CZ10 costs 29 cents.

NXP Semiconductors, www.nxp.com

Voltage-suppressor array meets lightning-surge requirements

Rated to withstand 100A surges typical in telecom Ethernet interfaces, the TClamp2502N 2.5V TVS array suits high-speed interfaces in applications with a high threat of lightning strikes. Integrating the vendor's EPD (enhanced punch-through-diode)-process technology with an advanced low-capacitance clamping architecture, the silicon-based device protects submicron transceivers against GR-1089-level lightning pulses. Available in a 2.6×2.6×0.6-mm SLP, the TClamp2502N 2.5V 100A protection device costs $1.44 (1000).

Semtech Corp, www.semtech.com

TISP surge protection meets European test requirements

In collaboration with LSI Corp—formerly, Agere Systems—the vendor designed the TISP surge protector using thyristor-overvoltage-protection technology. The device meets European ITU-T K.21 enhanced standards, requiring 600V rms, 600Ω, and 1A testing for 1 sec for the basic requirement, introducing significantly increased heating. The surge protector has a reduced protection voltage of 350 to 310V, ensuring that the 1-sec heating-effect test does not push the voltage over 350V. Aiming at modems, the device provides a 269 to 310V protection window. The TISP4310T3BJR-S surge protector costs 15 cents (20,000) or 12 cents (50,000).

Bourns, www.bourns.com

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BY RON TIPTON • TDL TECHNOLOGY INC

Mysterious data errors

DANIEL VASCONCELLOS

In the early 1990s, I was working as an engineer at White Sands Missile Range, NM. A contractor delivered a digital data-collection system that mostly worked correctly but put out garbled data at seemingly random times. The rack-mounted system comprised a number of approximately 5×5-in. PCBs (printed-circuit boards) that plugged into a card cage with a hand-wired backplane. Its developers designed and built it with the TTL (transistor-to-transistor logic) that was common at the time. The system received its power from a central, 5V, regulated supply.

We put up with the corrupted data for a month or so, and then the boss said to me, "Go fix it!" To the best of my knowledge, test equipment to troubleshoot this problem was not readily available at that time; at least, we didn't have any. So, I had to start by designing and building a way to monitor the incoming and outgoing data. I also built a data source that let me set any of the incoming 16 bits to either one or zero. It took more time to build the equipment than it did to find the problem! Whenever 12 or more of the incoming bits were ones, the ground bus on one PCB bounced up to about 0.7V. But the output error depended on which 12 bits were high.

The double-sided PCBs had a connector along one edge. A ground bus ran around the other three edges, but it was on only the bottom side and about 1/8-in. wide. The 5V bus on the top side ran down the middle of the board parallel to the connector side. It, too, was only 1/8-in. wide. As it turned out, the engineers who designed the system did an excellent job, but they apparently had little or no communication with the person who did the PCB design.

I fixed the problem using some solid, bare 12-gauge AWG wire, forming a three-sided loop, and continuously soldering it to the 1/8-in.-wide ground bus, making sure that it connected to all four ground pins in the connector. I did the same thing to the 5V bus. Apparently, only the one board was responsible for our errors. However, to be safe, I applied the same fix to the other boards.

THE ENGINEERS WHO DESIGNED THE SYSTEM DID AN EXCELLENT JOB, BUT THEY APPARENTLY HAD LITTLE OR NO COMMUNICATION WITH THE PERSON WHO DID THE PCB DESIGN.

This lesson was a useful one. Since then, I almost always design PCBs with a continuous ground bus around the outside edges. This bus is at least 0.2 in. wide on both sides of the board, and the two sides connect to each other with numerous vias. This approach goes a long way toward eliminating glitches in digital circuits and also helps lower noise in analog circuits. EDN

Ron Tipton is retired from White Sands Missile Range and is president of TDL Technology Inc (Las Cruces, NM). You can contact him at RTipton@tdl-tech.com.

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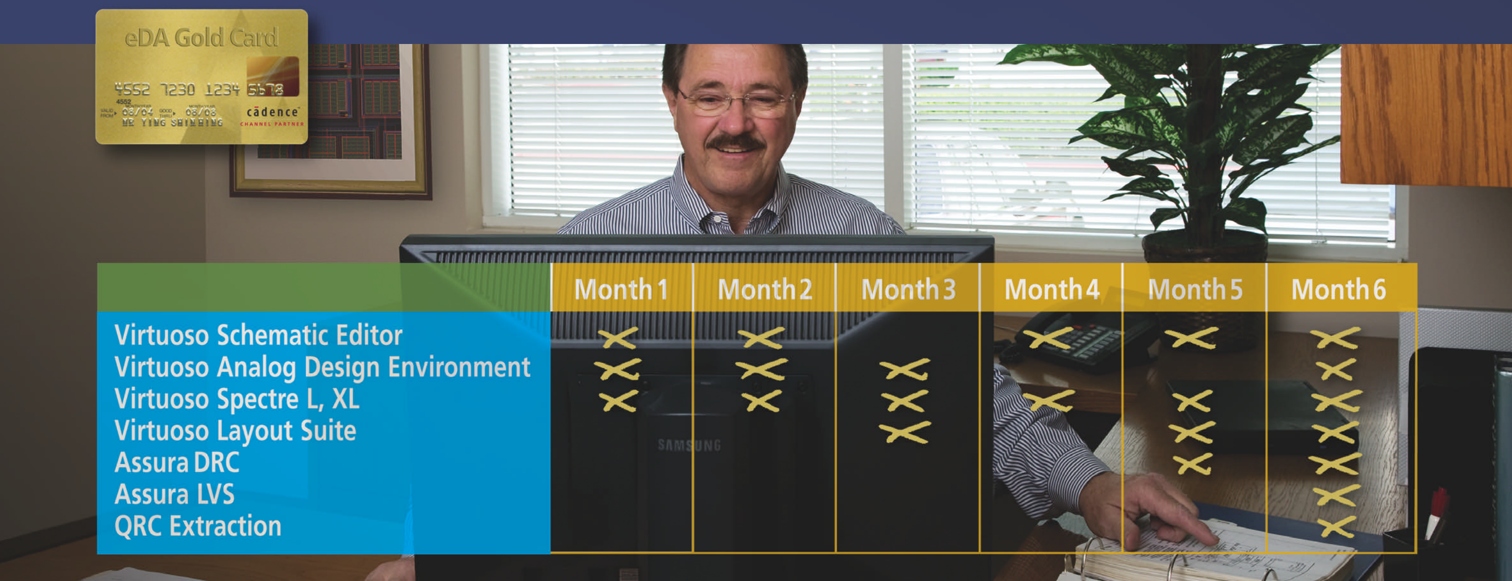

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